ELECTROSTATIC DISCHARGE WORKSHOP FOR ELECTRONIC AND IC INDUSTRY

Coordinated and Edited

by

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ORDERING NO ESD

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FORWARD

The field of Electrostatic Discharge (ESD) is getting more attention today, where once it was a knowledge for physicist and Electrical Engineers, the problems due to ESD on current high Technology products identified, requires that this knowledge be spread to all stratas of people manufacturing and using electronic products.

Awareness of this phenomena and practical application need to be set up to control and prevent the ESD problems resulting in long term cost saving to all parties concerned.

The EOS/ESD Association was set up recognising this need and thus it is the immediate objective of the Association to provide this awareness and educational needs, provide a neutral forum on ESD issues for vendors and users of ESD products or ESD sensitive products. Long Term the association hoped that she will be able to go into more technical services.

In the awareness and Educational Aspect, this workshop have been specially tailored. Many voluntary professional man-hours have been spent by the instructors to prepare for this workshop and I would like to thank them personally and on behalf of the Association for this dedication.

Finally, I would like to wish you all a happy and beneficial workshop.

C C LOO
CHAIRMAN
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CONTENTS

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1. BACKGROUND

The evolution and growth of integrated microelectronics coupled with associated problems of yield loss due to their high failure rates caused by charges brought on the surface the field of static electricity which lay dormant for centuries. This most ancient form of electricity was known to Greeks more than two thousand years ago. Electrostatics deals with electrical charges at rest whereas electronics deals largely with moving electrical charges. Charles D. Hendricks provided a comprehensive definition of electrostatics as "that class of phenomena which is recognised by the presence of electrical charges, either stationary or moving, and the interaction of these charges, this interaction being solely by reason of the charges themselves and their position and not by reason of their motion." This can be seen to be so from the fundamental definition of current, defined as rate of flow of charges. Historically amber is closely related with electricity. In fact the word electron, the basic unit of electrical charge, was derived from "elecktron", the Greek word for amber. Greek philosopher Thales, in 600 B.C., demonstrated the presence of the force of attraction when amber was rubbed. The work in this field, after Thales, progressed rather slowly. A chronological development of this field and the achievements made by the concerned scientists is given in Table 1.1: The work in the twentieth century mainly concentrated on the application and hazards of electrostatics.

In the present context we are mainly concerned with developing a systematic approach to understanding electrostatics, how it is generated, how it affects nature and man made surrounds. How to possibly eliminate its build-up and precaution to be taken, particularly, at various stages starting from material handling, manufacture to delivery and use of the finished device or system. Although the problems associated with electrostatics exist almost in every conceivable field but we will restrict our treatment only to electronics and IC industry related problems. The charge build-up in hospitals could be fatal if adequate care is not taken. It is therefore important for the manufacturers, of material and equipment for controlling and possibly eliminating ESD problem, to clearly understand the scope and the magnitude of this field. This can only be done by proper training of people and their understanding of the basic principles behind this form of energy which is generated free but can have crippling effect on our society.

There is no disagreement that the field of microelectronics, microcircuits and computers has virtually changed our lifestyle and the way we do our daily work. Most of it has been for the betterment of our standard of life, however, the latent problems were not fully recognised until premature failure of such devices with considerable yield loss, due to ESD, was known. Thus we need to know why such devices are so susceptible to ESD damage and what can be done to control the damage. Generally speaking the smaller the microelectronic device the greater is the chance that ESD can either completely destroy or set it on the path of gradual degradation to fail early in the operating life. Although the problem is known to be the most severe in the case of MOS devices but other type of devices are also affected.

What causes the damage is the build up of electrostatic charge. Therefore, if somehow the charge accumulation and storage can be avoided the problem can be completely eliminated, however, in general, it is not possible to do so. Hence the most possible alternative is to provide a path for the accumulated charge to be removed without affecting the device. This normally is done by providing a conducting path to ground. The question we need to answer now is what causes the accumulation of static charge. Tribological phenomenon is known to be responsible for static electricity.

Tribology is the study of the interaction of sliding/rubbing surfaces. It includes the following:

(1) Friction : characterised as a branch of physics

(2) Wear : characterised as a branch of material science or metallurgy

(3) Lubrication : characterised as a branch of chemistry

Table 1 : Chronological development of Electrostatics

'ear	Scientist	Origin	Achievements
00 B.C.	Thales	Greek	Demonstrated the presence of force of attraction when a cloth was rubbed with amber
600 A.D.	William Gilbert	British	Demonstrated that several other materials could attract light particles when rubbed with silk, flannel or fur etc.
672	Otto Von Guericke	German	Invented the first Electrostatic Generator (friction type machine) consisting of a sulfier ball which was rotated by hand against substances (silk, flannel or rubber) to create static charges.
700 early)	Francis Hauksbu	British	Built an electrostatic generator, using a rotating glass ball, capable of producing sparks and ionising the air.
704	Issac Newton	British	Discovered electric teledynamics.
729	Stephen Gray	British	Demonstrated that some materials can conduct or transfer static charges. Identified conductive and insulative properties of materials.
1746	P'Abbe J.A. Nollet and Charles Francois de Cisternay	French	Discovered the presence of two types of electrostatic charges, one produced by rubbing glass and second by rubbing resin. They also found out that similar charges repelled each other and opposite charges attracted each other.
1747	Benjamin Franklin	American	Demonstrated that glass and resin produced positive and negative charges when rubbed. He invented, that the lightning was electrical and that conducting rods would protect buildings from it. He also invented primitive electric motor.
1767	Priestly, Joseph Cavendish, Henry Robinson	British British	Produced the basis of the earlier experiments.
1775	Alessandro Volta	Italian	Invented the first induction-type electrostatic generator and in 1800 the first chemical electric battery.
1705	Charles Augustin de Coulomb	French	Coulomb's law of electric attraction.
1785	Abraham Bennet	British	Invented gold leaf electroscope.
1811	Poisson, Simeon-Denis Green, George Gauss, Carl Friedrich	French British German	Detailed theoretical treatment of electrostatics.
1831	Michael Fraday	British	Introduced the concept of electrostatic lines of force surrounding the charged bodies.
1864	Maxwell, James Clerk	British	Relations of electromagnetic field.
1878	C F Varley James Wilnhurst	British	Discovered the modern electrostatic generators.
1930	Van de Graff, R.J.	American	Discovered the friction type electrostatic generator.

It is known that upto 39 to 48% of the IC reject can be due to ESD alone[2]. This figure should be seen in the light of expected MT BF of about 10 to 100 FITs (10 to 100 failure in 10^9 device-hours). Apart from the direct yield loss resulting in poor return on capital the warrantee cost due to ESD failures is normally very high. It, therefore, makes sense to invest in implementing an effective ESD control programme. This will not only increase the productivity but will also enhance corporate's image as a leader in maintaining high reliability standards. This will create a feeling of goodwill and trust, two vitally important factors for expansion and economic success of an enterprise.

Tribology is a complete interdisciplinary subject and has suffered the same neglect as have other such subjects. Rubbing two materials together or separating them from one another causes tribo-electrification. This was demonstrated by Thales as far back as in 600 B.C. The magnitude of the charge is highly dependent upon the particular materials' propensity towards giving up or taking on electrons. Some substances readily give up electrons, while others tend to accumulate them. Dissimilar materials are particularly susceptible, especially if they have high surface resistivity.

Another way of placing a static charge, positive or negative, on a body is by induction which could be caused by placing a body in close proximity to a highly charged object. This can be shown by using classical gold leaf electroscope.

Accumulation of static charges is the property of non-conducting materials as the stored charges are unable to move because of poor electrical conductivity. The polarity of charge acquired by different materials when rubbed, brought together or separated from one another is given by Triboelectric series given in Table 1.2. The materials higher in the series labeled "positive" take on a positive charge every time they come in contact with a material lower in the series. The magnitude of the charge developed is roughly related to the relative position of the materials in the series.

TABLE 1.2 – TRIBOELECTRIC SERIES

Triboelectricity can be generated by two pieces of the same material. For example the interior of a plastic bag may produce enough charge, when opened, to damage a sensitive electronic component as it is dropped into the bag.

Thus two materials near one another will produce less static electricity than materials widely separated in the series.

2. ECONOMIC CONSIDERATIONS OF ESD

It is now normally accepted that to reduce the early failures, to reduce the warranty cost, the devices should be subjected to static/dynamic burn-in test. Managers now understand that in the long term it pays to invest in installing a suitable system for test. Although, electrostatics had been around for a long time still people do not believe and understand that the introduction of an effective programme to control ESD damage would be economical. In the first instance not everyone is convinced that a particular type of failure is due to an electrical discharge. To fully understand the economics of an ESD programme, it is essential to know the factors which affect the charge build up. We now know that increasing the conductivity must surely help reduce the problem. How this concept is used in developing suitable material will be seen later?

The economics of ESD can be worked on the similar basis as for the burn-in. 10:1 rule of cost of testing would apply in this case as well. The procedure to be adapted is to estimate the cost of the device with and without the introduction of the ESD programme. Profit (if any) on the yearly basis is calculated taking into consideration the cost of equipment, material and training etc. The break-even point can be found by calculating the yearly saving.

At this stage of our investigation it will be enough to have a feel of the extent of the problem. The evaluation of the direct cost will largely depend on the hazards involved. In situations where human life could be at risk due to ESD, the cost evaluation becomes, to a large extent, subjective, emotional and often political issue. What is the cost of a human life has been a topic of debate for a long time? Insurance companies tend to assess the cost of life differently at different times. It is now known that, in a number of fatal accidents reported in the past, ESD was identified as the main cause. To prove the point under discussion some examples are now considered. For a very long time people knew from experience that ESD can cause explosion of fuels and ammunition. For example in 1937, the German flying boat Hindenburg, a vessel inflated with hydrogen instead of helium, caught fire while landing in Lakehurst, New Jersey and resulted in the death of 38 of its hundred or 50 passengers. ESD is understood to be the cause of explosion and fire. The cost of the vessel can be easily estimated but the true and realistic estimation of the cost of lost human lives, keeping in mind the plight of the families affected, can never be totally satisfactory. Yet another tragic example of damage due to ESD is the ignition of the rocket by induction of about 28,000 volts on its igniter squib in 1964. This resulted in the death of three technical personnel while injuring eleven others. In this accident the eastern test range laboratory at Cape Canaveral in U.S.A. was totally destroyed. The built-up of static charge was due to a synthetic fibre (polyethylene) drape, used as a dust cover for a Thor Delta third-stage solid-propellant rocket.

The examples of damage due to the discharge of accumulated charge in nature (lightning) are numerous. Only recently an airport in Australia was hit by lightning damaging the airport and causing inconvenience to passengers. Thus it can be concluded that the cost of damage, due to static charges, could be very high. It is therefore important to know and understand how to control it and possibly reduce the cost.

More importantly in manufacturing sector particularly in electronic and IC industry static electricity creates problems in two ways:

(I) Yield reduction due to total failure of the devices/sub-assembly/assembly and sub-system/systems.

(II) Increased warranty cost due to the use of ESD degraded units.

The cost of total or catastrophic failure becomes obvious rather quickly, however, the cost of failure due to reduced MTBF of degraded devices can only be assessed after sometime. ESD sensitive devices are being used in variety of equipment. While the failure of such devices in cheap toys or household appliances may be tolerated the same cannot be true certainly for their failure in a spacecraft or life saving medical equipment. So what is essential is to implement ESD elimination and control programme to suit the need and economic requirements.

COST OF ESD DAMAGE

In this section attempts are made to estimate the cost of ESD damage resulting in yield loss. Percentage yield loss in this case is defined by equation [2.1]

$$\% \text{ Yield loss due to ESD} = \frac{\text{Number of failures due to ESD}}{\text{Total Produced}} \times 100 \qquad [2.1]$$

Example:

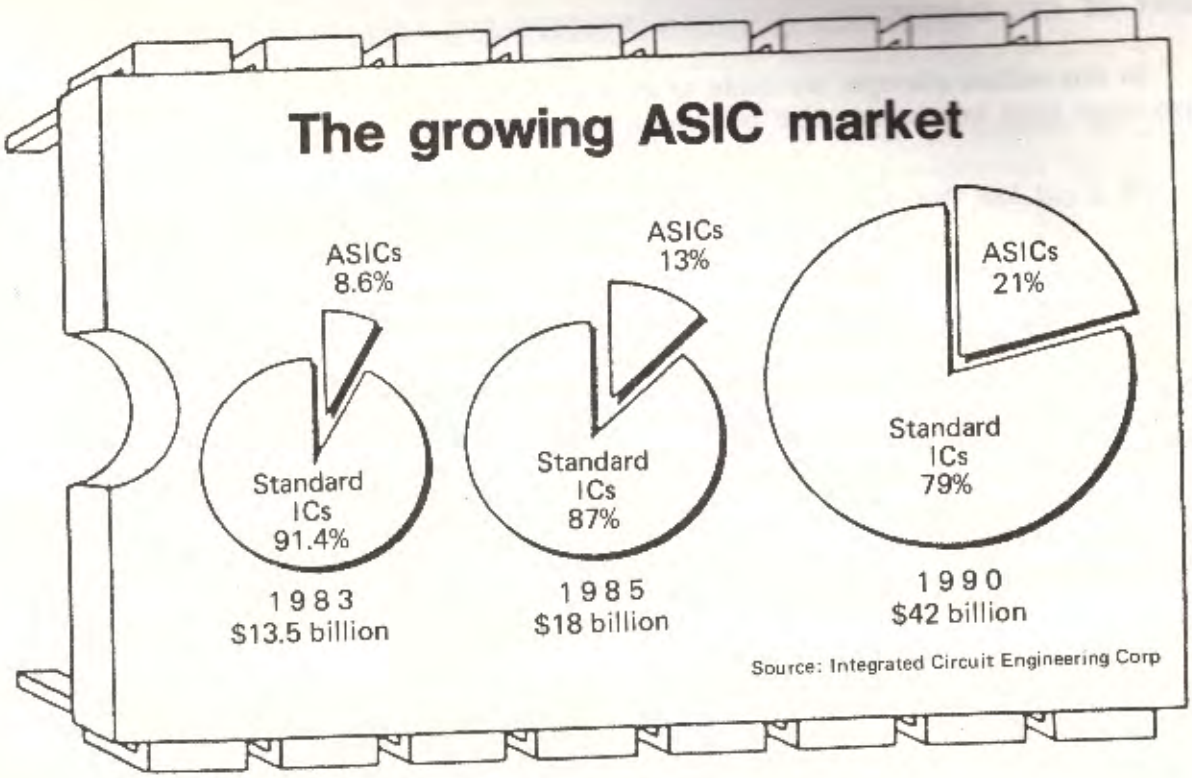
Let the % yield loss due to ESD = X
Let the cost of individual units = P
Let the Average number of units produced per day = N

$$\text{Pure loss per year} = \left[\frac{X}{100} \times N \times P\right] \times 365$$

The cost of an ESD sensitive device can vary from few cents to a few hundred dollars. The global production of such devices is steadily rising day by day. The value of x in the above can be between 3 to 30, depending upon the degree of ESD control programme being implemented. Thus the overall global loss, due to total failure of devices, each year could be billions of dollars. In April 1984 G.C. Quin, technical editor of Electronics Test Magazine reported that:

"The volume range of ESD sensitive components is rising faster than the development and usage of ESD protections . . . . . Estimating costs of ESD failures not caught at manufacturing inspection is far more difficult. Many of the degraded, walking wounded devices may not show up until after termination of the manufacturer's guarantee".

It is reported that implementation of an effective ESD programme by lockhead reduced the ESD failures by a factor of sixteen. In 1980, this resulted in a cost saving of US$1.8 million. This reduction in ESD failure does not tell the exact percentage failure occuring even after the implementation of the programme. Even after the introduction of an effective ESD control programme the failure of ICs could be in the range of 39 to 48%. The projection for the IC industry for 1990 is that worldwide ICs worth US$42 billions will be produced. Taking an overoptimistic percentage of catastrophic failures due to ESD as only 2%. The real loss would be US$0.84 billion. The picture of growing IC market is shown in Fig 2.1[3]. So far we have discussed only the cost, of not implementing an ESD programme, due to yield reduction via total or catastrophic failures. At this stage it is important to have an idea about the cost of equipment, material and staff training in implementing the ESD control programme. The cost will largely depend upon the degree of protection being considered to adequately protect the units being produced. For a particular company making use of ESD sensitive devices for their products, the capital investment in 1985 was approximately US$25,000.00. The breakdown of this cost is given in table 2.1



(a)

(b)

Fig. 2.1 – Growing I.C. Market

Table 2.1 – Cost of Implementing An ESD Control Programme

Items	Cost
	US$
Air ionisers	10,000
Conductive floor mats	5,500
Field scanners	3,250
Resistivity meter	2,250
Wrist strap @ US$12.00 per piece	600
Antistatic bags	250
Conductive bags	150
Antistatic solder suckers	2,500
Static monitor	500

A MODEL FOR ESTIMATION OF WARRANTY COST DUE TO ESD DEGRADED DEVICES

The use of degraded devices which get through the test procedure are bound to fail permaturely anywhere between the assembly line and the field. Under this situation the usual 10:1 rule of cost of testing would apply and the pattern of escalating cost of testing would be as shown in Fig. 2.2. It is therefore important to stop such wounded devices getting out of the factory. This can only be done by suitably implementing an ESD control programme.

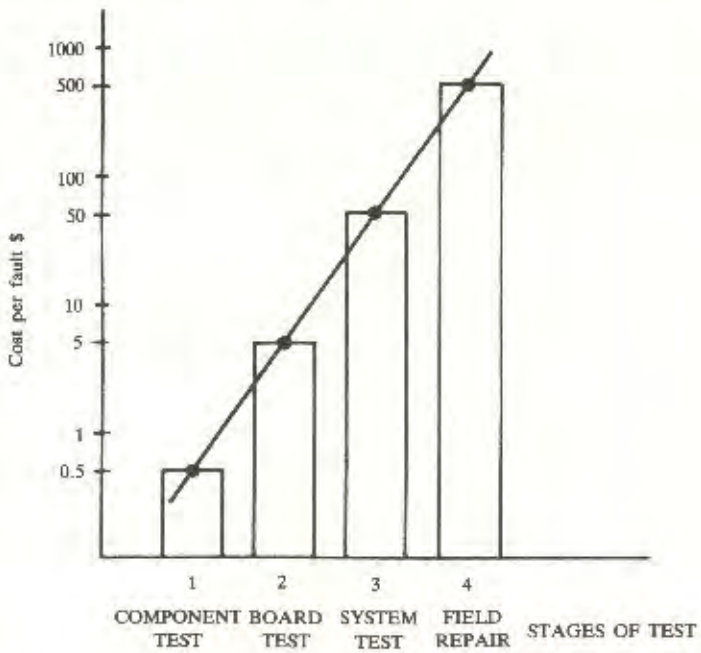


Fig. 2.2 – 10:1 Rule of Cost of testing

To justify the investment in implementing an ESD control programme we now proceed to calculate the return on investment through yield improvement. The ratio of total investment to yearly saving will determine the break-even period for the investment. This period could be anything between few months to couple of years depending upon the actual failure rates before and after the implementation of the ESD control programme.

The yearly saving due to the introduction of an ESD control programme is given by equation [2.2].

$$\text{Yearly Saving, } YS = N(R_1M_1 + R_2M_2 + R_3M_3)(\lambda_1 - \lambda_2) \qquad [2.2]$$

where

N Total number of dervices produced per year

λ_1 Failure rate prior to the introduction of the ESD programme

λ_2 Failure rate after to the introduction of the ESD programme

R_1, R_2, R_3 % total failure rates occuring at board test, system test and in the field

M_1, M_2, M_3 cost of repair at board, system and field level.

The main assumptions of equation [2.2] are:

(1) R_1 R_2 and R_3 remain the same during two situations

(2) $\lambda_2 < \lambda_1$

The break-even period for the investment can be calculated from equation [2.3].

$$\text{Break-even period} = \frac{\text{Investment}}{\text{Y. S.}} \qquad [2.3]$$

SOME EXAMPLES

Reporting on the high cost of ESD damage Harris Semiconductor, Melbourne, U.S.A. revealed that 28% of the total field failures were clearly identified to be ESD induced. Additional 44% of the failures may have been ESD – induced because the exact cause of their failures could not be positively identified. Dick Moss of H.P. reports that upto 25% of the total field failures could be caused by ESD. The average warranty cost per months for a product was US$40,000. This means that the average warranty cost per month due to ESD failures alone would amount of US$10,000. These two examples suggest that to keep the cost down ESD must be controlled.

The last example in this case comes from Teradyne corporation. These figures were revealed at a recent industry conference in Cherry Hill, N.J. A system contained five boards full of ESD sensitive devices. Each board used 20 such devices. ESD induced failure rate of the devices was 0.5%. Following calculations show that this would amount to system failures rate of upto 50%:

Device failure rate 0.5%

$\therefore$ Board failure rate $\frac{0.5}{100} \times 20 \times 100 = 10\%$

$\therefore$ System failure rate $\frac{10}{100} \times 5 \times 100 = 50\%$

To account for this loss the company would need to produce more. This amounted to additional cost of production per year of US$600,000 to overcome these static induced failures. If the realistic after tax profit is 5% then it would take US$12 million in additional sales a year just to breakeven.

It must be noted that the above calculation of cost does not take into consideration the loss due to poor publicity via unsatisfied customers. This also does not take into account any hazardous situations arising directly due to ESD, such as reported earlier.

3. WHAT IS RED ?

In the last chapter it has been concluded that to keep the cost down ESD must be controlled. To be able to do so it is essential to know what ESD is. Most simply ESD is the discharge of static electricity. The branch of electricity dealing with static charges is known as Electrostatics. Therefore, understanding of electrical charges and their interaction with other objects is necessary. Static electricity is an excess or deficiency of electrons on one surface with respect to another surface or to ground. A surface is said to be negatively charged if it contains an excess of electrons which we know carry a negative charge. An electron deficient surface is said to be positively charged. The static electricity is measured in terms of voltage (volt) and charge in terms of coulomb.

A surface gets charged when the molecules are electrically imbalanced. Electrostatic discharge (ESD) takes place when a re-establishment of equilibrium is attempted through the transfer of electrons between one object and another that is at different voltage potential.

GENERATION OF STATIC CHARGE

The most common way of generating static electricity is triboelectrification. However, it is not necessary that surfaces must rub against each other for static charges to build up. This can occur even when two different materials in contact are separated. It can be shown that static voltage in the range of 2 to 6 kV can be generated through this process. The true mechanism of formation of charge is rather complex, but the main factor is the transfer of electrons.[4] The magnitude of the charge is dependent on the propensity of the material towards giving up or taking on electrons. This is also greatly influenced by the relative humidity in the air and the conductivity of the material. The generation of static charges when two materials are separated is shown in Fig 3.1.

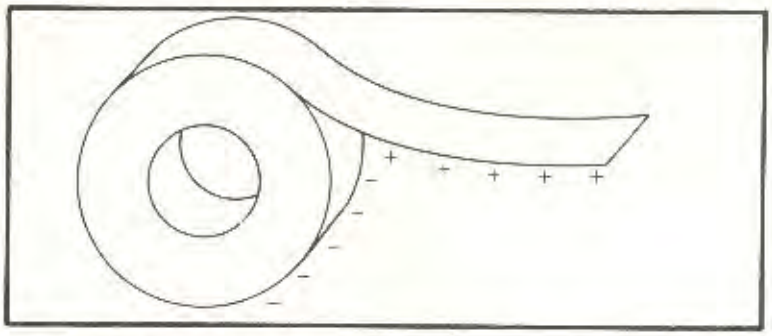


Figure 3.1(a) – A strip of acetate tape is attracted to the surface of the tape reel. Two insulating materials of the same nature can develop opposite charges if enough friction is applied.

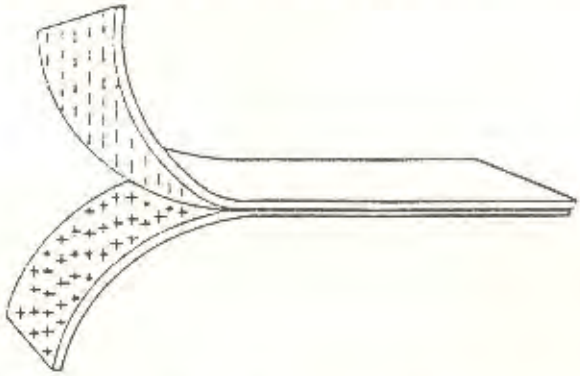


Figure 3.1(b) – Static Charges caused by contact and separation of materials.

In the manufacturing environment the biggest source of electrostatic generation is the workers and their movement. It is no surprise then that most semiconductor manufacturers are looking for factory automation by reducing the extent of man-machine interface. Particularly in IC industry this is being attempted by introducing the concept of computer aided quality assurance in which the functions of testing on the production line and random sampling inspection by Q.A. staff are performed in one step. Some of the prime sources of static generators as reported in a manual[5] are given in table 3.1.

Table 3-1. Prime Sources of Static Electricity in an Electronics Work Area.*

Sources	*Contributors to High Static Generation*
People	Walking, rocking in a chair, getting up from a chair, putting on and removing work smocks, any brisk or repetitive motion.
Clothing	Clean room smocks, synthetic shirts, sweaters, pants, etc.; shoes with synthetic (such as, neoprene, foam rubber) soles, heels, and innards.
Chairs, work stools	Vinyl covered, fiberglass, finished (such as, varnished, shellacked, polyurethane coated), waxed.
Workbench tops	Plastic, vinyl, covered, finished, waxed.
Floors	Vinyl, finished wood, sealed concrete, waxed.
Parts bins, trays, tote boxes	Plastic, finished wood or metal.
Packaging material	Plastic foam, bubble pack, cushioning, polyethylene bags, vials, containers, Styrofoam pellets (shells, peanuts).
Tools	Plastic solder suckers, hand tools (coated handles), soldering irons (with ungrounded tips), heat guns (used for heat shrink tubing, drying conformal coating, etc.), solvent brushes (synthetic bristles).
Manufacturing equipment and processes	Drying ovens, degreasers, sandblasters, temperature chambers, solder flow machines, integrated circuit handlers or loaders, spray conformal coating, potting, spray painting and cleaning, fault isolation with cryogenic sprays;

GENERATION OF STATIC CHARGES IN NATURE

Electrostatic discharge phenomenon in nature, within the atmosphere, occurs in the form of lightning flash. Such flashes are usually associated with thunderclouds but are also known to have taken place in other situations such as in the erupting gas of an active volcano[6]. The flash occurs as a consequence of restoring charge equilibrium within clouds (cloud to cloud discharge), between a cloud (intracloud discharge), between a cloud and air (air discharge), or from cloud to the ground (ground discharge). The neutral molecules of moving clouds get separated into a store of accumulated positive and negative charges. The mechanism of the natural electrostatic discharge phenomenon is fairly complex and its detail treatment would be out of place. It causes extensive damage and attempts are made to reduce the damage. The sequence of events leading upto the lightning are shown in Fig. 3.2.

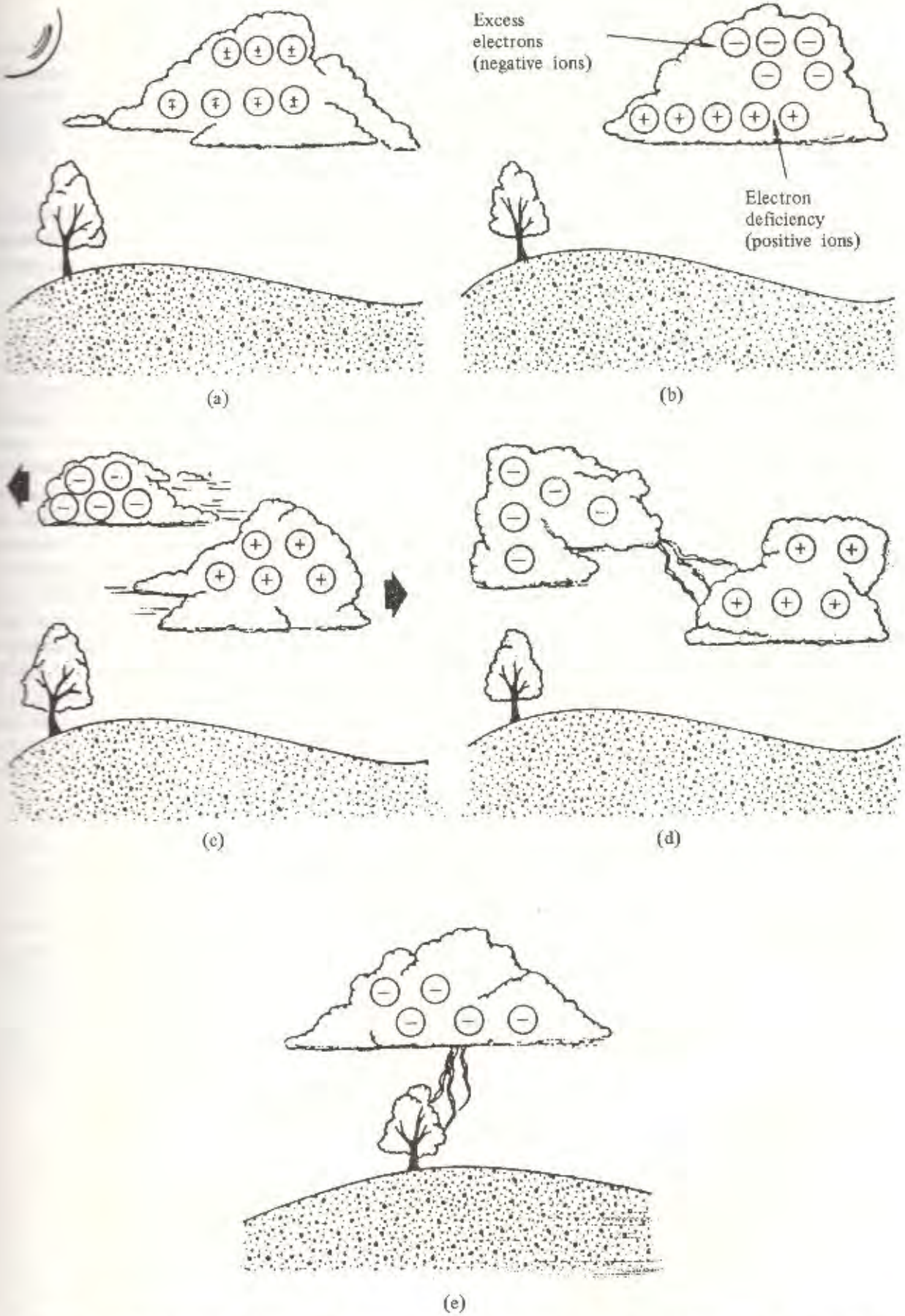


Figure 3.2 – Static electricity in nature: (a) electrically neutral cloud (b) charge separation; (c) cloud separation; (d) lightning between clouds; (e) lightning to earth.

PROTECTION AGAINST NATURAL ELECTROSTATIC DISCHARGE

Surprisingly the method of protection provided for lightning flashes, by Benjamin Franklin in 1752, has undergone practically no change. The protection system is based on sound fundamental principles and clear understanding of lightning flash mechanism. The purpose of the lightning rod and conductive path to ground is to intercept a lightning discharge before it can contact a building and pass the lightning current, the peak value of which may be up to 20,000 Amperes, safely to ground.

It is of interest to note that the ESD protection circuits and systems designed to protect ESD susceptible devices and equipment are based on the same principle as used by Benjamin Franklin. The principle being the path diversion of devastating electrostatic discharge so as to eliminate the damage.

PEOPLE AND ELECTROSTATIC DISCHARGE

People living in cold climatic country where the relative humidity is generally low often feel a gentle kick when they hold a metal knob to open the door after having walked on a synthetic carpet. The kick is due to the discharge of the accumulated charge on the body generated as a result of rubbing action between the foot and the carpet. This is normally felt when a person is charged to 3,500 to 4,500V. It is therefore relatively simpler to convince them that ESD does exist. However, the same is not true for tropical countries where the relative humidity is normally very high and the use of synthetic carpet is not common. Since ESD cannot be easily seen, people do not believe that it can be a killer. Hence one of the main problems in eradicating the ESD induced damages lies in training and educating almost everyone in electronic and semiconductor industries. It will serve little useful purpose if the retailers, service personnel, commercial and marketing people were not adequately informed. I have seen in the U.K., India and most recently in Singapore that ESD sensitive devices are picked by hand, counted and packed in an ordinary polyethene bags. How can a ESD control programme in such situations achieve the desired objective? The message we get from such observations is that the ESD control and protection programme must be total, comprehensive and above all effective.

4. PHYSICS AND PRINCIPLES OF ELECTROSTATICS

For a comprehensive understanding of how to deal with electrostatic problems it is necessary that mathematical treatment of static electricity is done in such a way that enforce the physical understanding. This means obtaining relations between various parameters which involve geometrical configurations of conductors and dielectrics, the distribution of charges on the conductors and in the dielectric medium separating them, the potential differences between conductors, and the field distribution. This will mean a clear understanding of capacitance and its behaviour under different operating conditions. In dealing with ESD problems most of the time the ultimate equations are reduced to charging and discharging characteristics of capacitors.

ESD is essentially establishing a condition of equilibrium so as to create a neutral matter. For this we need to understand the polarising nature of matter and the physical nature of charge. The understanding of laws controlling the interaction between the charge objects is essential to calculate the energy requirements. It is also necessary to know how the presence of charge affects the other objects in its neighbourhood.

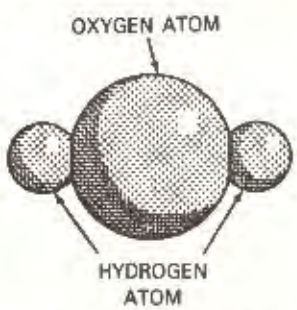
THE CHARGE

To understand static electricity it is essential to differentiate between positive and negative charges. Electrical charge (Q or q) is not a derived entity but rather a matter with unique properties. It is measured simply as a number of charge particles, one unit (coulomb) of charge being equal to about 6.25×10^{18} particles of charge. It is well known that electrical particles have their own mass and charge.

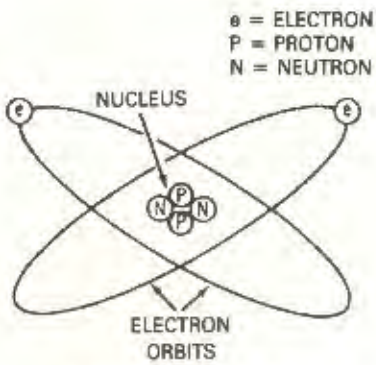
The microscopic picture of a material consists of assembly of molecules which in turn are made up of atoms. Under equilibrium condition, in the absence of external forces, an atom remains electrically neutral. In this situation the total number of electrons carrying negative charge in various orbits is exactly balanced by equal number of protons, carrying positive charge at the centre of the atom. Therefore, the net charge seen from the outside is zero.

Water molecule consisting of hydrogen and oxygen atoms and a helium atom consisting of electrons, protons and neutrons is shown in Fig 4.1. The situation for other atoms will be similar to helium i.e. the number of electrons, protons and neutrons will be the same. An atom as shown in Fig 4.1 is said to be in its normal, balanced, or neutral state. This balanced state can be disturbed if some force is acted upon the atom in such a way that either electrons are removed from, or added to, the atom. The removal of electron will make the neutral atom positively charged and its addition will do the reverse. This process is known as ionization and the charged atom is called an ion.

In an atom the positive charge of proton is exactly equal to the negative charge of electron. The electrons are kept in their orbits due to the electrostatic force between the positive charge, at the nucleus, and the orbiting negative charges.



The water molecule.



The helium atom.

Fig. 4.1 – The Structure of a water molecule and helium atom.

A PROTON B ELECTRON

Fig. 4.2 – Field associated with protons and electrons.

The Law of Electrical Charges: The starting point in the mathematical study of electrostatics is Charles A. de Coulomb's experimental law. This gives the force between two electric charges in an infinite isotropic medium. The law includes the following information:

- Similar charges repel and opposite charges attract.
- Force between the charges is proportional to the product of charge magnitudes.
- Force in inversely proportional to the square of the distance between the charges.
- Force is dependent on the medium in which the charges are placed.
- Force acts along the line joining the charges.

The above information can be represented by the equation [4.1]

$$\bar{F} = \frac{Q_1 \; Q_2}{4\pi\epsilon_o d^2} \; \bar{a}_r \qquad [4.1]$$

where $\bar{F}$ = force in the direction of unit vector $\bar{a}_r$, newton, N

Q_1 and Q_2 = magnitudes of the charges, coulombs, C

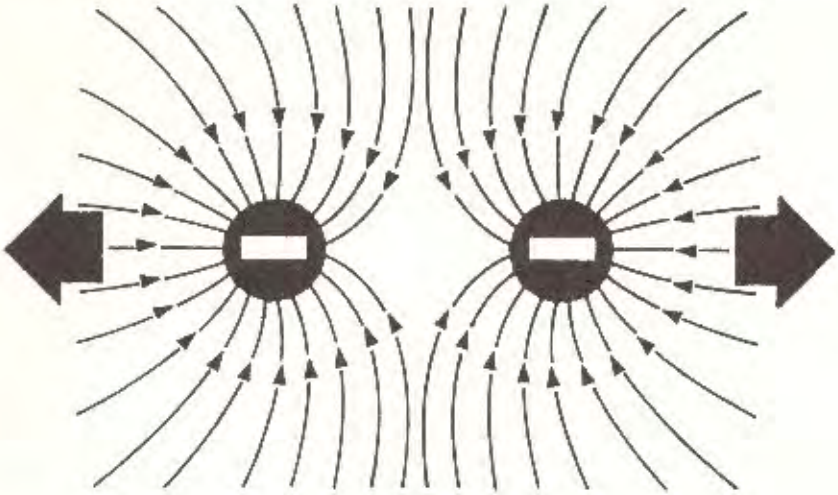
ϵ_o = permittivity of free space.

d = distance between the charges, metre, m

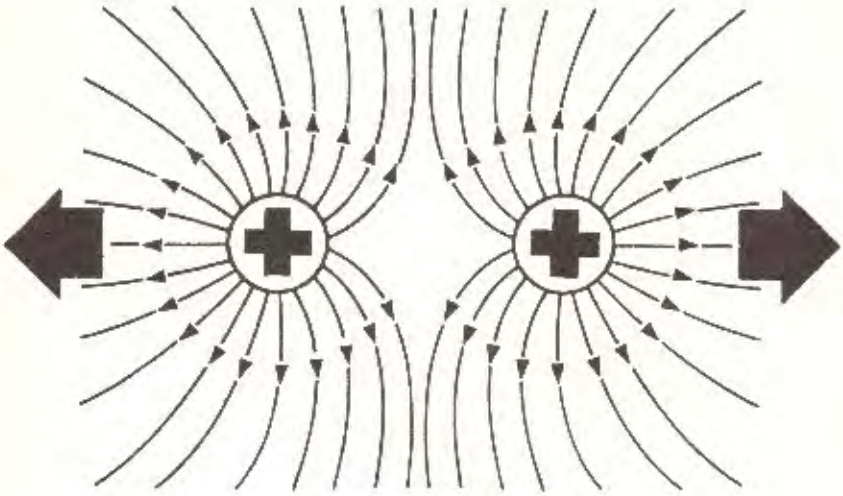
Equation [4.1] applies only to charged bodies whose dimensions are small compared to distance between the charges. Professor R. A. Waldron[7] of Ulster Polytechnic suggests that equation [4.1] applies only in limited cases under suitable conditions. However, the equation [4.1] can be generalised if an additional term is included to account for the velocity of one charge relative to the other as given by equation [4.2]

$$F_w = \left(\frac{Q_1 \; Q_2}{4\pi\epsilon\epsilon_o \, d^2}\right)\sqrt{1 + \left(\frac{v}{c}\right)^2} \qquad [4.2]$$

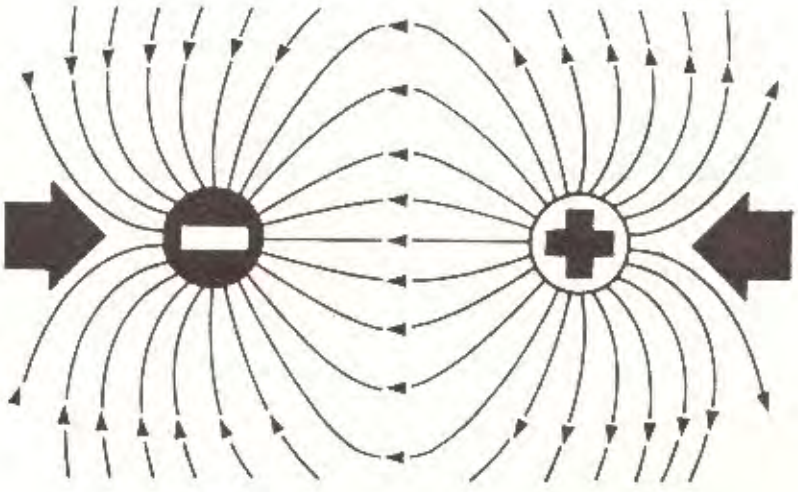
The entire region in which the presence of an electric charge can be experienced is called its electric field, and its magnitude is specified by a quantity called electric field intensity $\bar{E}$. The field lines always originate at the positive charge and terminate the negative as shown in Fig 4.2. The interaction between these lines as governed by coulomb's law is shown in Fig. 4.3. The electric field or electric field intensity E at a point is defined as the electric force per unit charge on a positive test charge. The test charge should be such that does not disturb the charge distribution of the system. Like force E is a vector quantity. By definition E in air due to a charge Q is given by equation [4.3].



A ELECTRONS REPEL



B PROTONS REPEL



C ELECTRON AND PROTON ATTRACT

Figure 4.3 – Interaction Between Field Lines

$$\bar{E} = \frac{\bar{F}}{q} = \frac{[Q\ q/4\pi\ \epsilon_o\ d^2]\ \bar{a}_r}{q} = \frac{Q}{4\pi\ \epsilon_o\ d^2}\ \bar{a}_r \qquad [4.3]$$

For a system of point charges, the total field is found by integrating equation [4.3] to express the electric field. This actually amounts to vectorial sum of electric field due to all the point charges. This is given by equation [4.4].

$$E = \frac{1}{4\pi\epsilon_o}\int \frac{\bar{a}_r}{d^2}\ dQ \qquad [4.4]$$

The units of $\bar{E}$ in mks system as in equation [4.3] is Newtons/coulomb. However, a more convenient and practical approach to express $\bar{E}$ is in terms of the potential difference between the objects divided by the distance between them. This approach is useful in calculating electric field between the two parallel plates of a capacitor. In this case the field is expressed as volts per metre.

TO SHOW THAT THE FIELD IN NEWTONS PER COULOMB IS THE SAME AS THE VOLTS PER METRE

The work done in moving a charge Q, located at a point on the line of force, in the direction of the electric field through an incremental distance dl will be QE dl and this equation for a finite distance can be expressed by equation [4.5].

$$dw = QE\ dl$$

$$\text{or} \quad w = QE\int dl \qquad [4.5]$$

This situation is shown in Figure 4.4

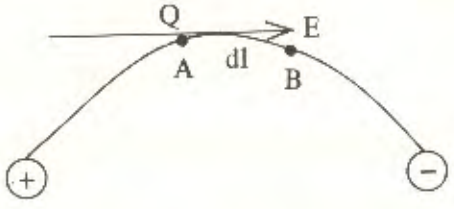


Fig. 4.4 concept of field

Potential is a derived entity. The difference in the potential ($V_B - V_A$) of a charge Q at position A and B is the work done in moving it from A to B and is given by equation [4.6]

$$W = Q\ (V_A - V_B) \qquad \text{Joules}$$

In this case it is assumed that $V_A > V_B$

$$\therefore \quad QE \int dl = Q\ (V_A - V_B) = -\ Q\,dV$$

$$\text{or} \quad E = -\frac{dV}{dl} \qquad \frac{\text{Volt}}{\text{Metre}} \qquad [4.6]$$

The significance of the negative sign being that the work done is positive when the charge is moved up the potential gradient i.e. from a point of lower to one point at higher potential.

Now let us consider the materials which are most likely to get polarised by either gaining or losing electrons. The condition of charge equilibrium will always exist in metals because of its conductivity and high mobility of electrons. This means no significant static field will exist between different points of the same mental. In non-conductive materials, however, because of lower electrical conductivity due to lower electron mobility rapid equalisation of charge imbalance is not achieved. Thus nonconductors are known to get positively charged by losing electrons when rubbed. To avoid build up of static charges the electrical conductivity should be increased.

Components or systems sensitive to static electric field can be damaged if subjected to high enough electric field intensity. In particular MOS devices are vulnerable to this due to their SiO_2 layer. The breakdown field of SiO_2 is approximately 6×10^6 v/cm. Thus a 500 Å SiO_2 layer device will fail at 30V.

ELECTROSTATIC SHIELD

The concept that a metal cannot be ionised because of its high electron mobility is used to construct electrostatic shield. A static field cannot exist within a conductive enclosure. This knowledge can be used to protect ESD sensitive devices by keeping them in conductive bags or other suitable containers. The principle of designing a shield or a shielded conductive container to protect ESD sensitive device is similar to one used to resolve the electromagnetic interference (EMI) problems. For a comprehensive knowledge on the principles and applications of shields one can refer to the book by Donald R. J. White[8] or more specifically on shield evaluation, a paper by Faught[9]. How an ESD sensitive device is protected inside a conductive bag and damaged when placed in an insulating bag is shown in Fig. 4.5.

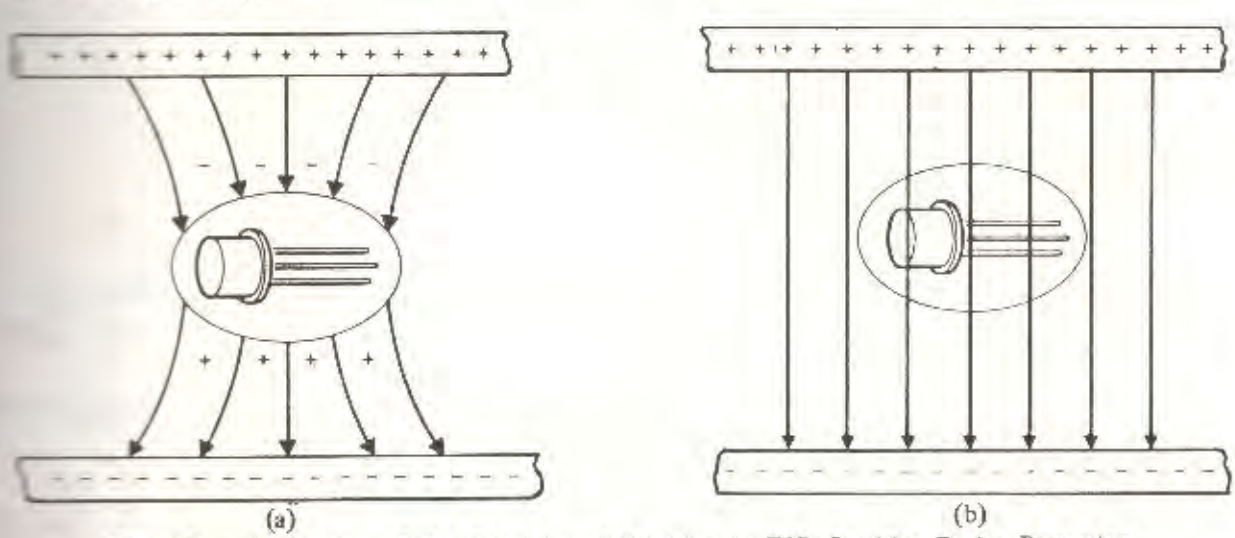


Fig. 4.5 – Application of the Principles of Shielding in ESD Sensitive Device Protection.

ROLE OF CAPACITANCE IN ELECTROSTATICS

Capacitance is the most important single electrical components which plays a vital role in electrostatics. It's clear understanding is essential in dealing with ESD related problems. From equation [4.6] the potential difference between charge carrying conductors will be given by equation [4.7].

$$V = -\int E \, dl \qquad [4.7]$$

It can be concluded that the potential difference V will be proportional to Q as E according equation [4.3] is known to be proportional to Q. It is known that the ratio of charge to potential difference of a system is constant and depends only on geometry of the conductors and the medium in which the lines of force exist. This situation can be represented by the equation [4.8].

$$\frac{Q}{V} = C \qquad [4.8]$$

This constant is known as capacitance. The above expression is also applied to an isolated conductor but in this case infinity is taken as the reference level of potential. With Q expressed in coulomb and V in volts, C is given in farads (F). It can be shown that the capacitance is proportional to the first power of the linear dimension. In case of a sphere of radius R filled with a material of permitivity ϵ the capacitance is given by equation [4.9].

$$C = 4\pi\epsilon\epsilon_o R \qquad [4.9]$$

PARALLEL PLATE CAPACITOR

If we assume that an isotropic homogeneous dielectric material is supported on either side by conducting plates in such a way that uniform electric field is contained within the plates (area of cross section A) separated by a distance D then the capacitance is given by equation [4.10].

$$C = \frac{\epsilon\epsilon_o A}{D} \qquad [4.10]$$

In this the field strength between the plates (E) is given by the ratio of the surface charge density ($\sigma_s = Q/A$) and $\epsilon\epsilon_o$

$$\therefore \quad \sigma_s = \frac{Q}{A} \quad \text{or} \quad E = \frac{\sigma_s}{\epsilon\epsilon_o} = \frac{Q}{\epsilon\epsilon_o A} \qquad [4.11]$$

$\therefore$ Potential difference between the plates V = E.D

$$V = \frac{Q}{\epsilon\epsilon_o A} D$$

$$\therefore \quad C = \frac{Q}{V} = \frac{Q}{Q\,D} \quad \epsilon\epsilon_o A$$

$$C = \epsilon\epsilon_o \frac{A}{D} \quad F \qquad [4.12]$$

If the medium separating conducting plates is air for which $\epsilon = 1$

$$C_o = \epsilon_o \frac{A}{D} \quad F \qquad [4.13]$$

Aguet[10] has related the propensity of material towards ionisation in terms of σ_s given by equation [4.14].

$$\sigma_s = 15 \times 10^{-6} \left[(\epsilon_r)_1 - (\epsilon_r)_2\right] \quad \frac{C}{m^2} \qquad [4.14]$$

where $(\epsilon_r)_1$ and $(\epsilon_r)_2$ is the relative permittivity of two materials. This relationship can be used to estimate the electrostatic voltage generated during normal working within an industrial environment. Conversely using the measured values of the electrostatic voltage and parallel plate capacitor model one can calculate foot to floor capacitance during normal walking. Unger[11] has measured the average voltage generated during normal walking across a carpet to be about 15,000 V. Assuming the average area of rubber sole shoe in contact to be 300 cm^2 and relative permittivities of synthetic carpet and rubber to be 5.5 and 2.0, we calculate below the charge stored and the electrostatic voltage generated.

$$\sigma_s = 15 \times 10^{-6} \ (5.5 - 2.0)$$

$$= 5.25 \times 10^{-5} \ \frac{C}{m^2}$$

$$Q = \sigma_s \times A = 5.25 \times 10^{-5} \times 300 \times 10^{-4}$$

$$= 1.575 \times 10^{-6} \text{ coulombs}$$

$$V = 15 \times 10^3 \text{ V} \quad \text{(measured)}$$

$$C = \frac{Q}{V} = \frac{1.575 \times 10^{-6}}{15 \times 10^3}$$

$$= 105 \text{ pF}$$

The electrostatic energy stored in the capacitor of charge Q is given by equation [4.15].

$$\text{Electrostatic potential Energy } E_c = \frac{CV^2}{2} \qquad [4.15]$$

In the above example

$$E_c = \frac{1}{2} \times 105 \times 10^{-12} \times (15 \times 10^3)^2$$

$$= 0.0118 \text{ Joule}$$

$$\text{or} = 11.8 \text{ mJ}$$

For practical applications and calculations the values of the electrostatic voltages reported by Unger[11] are reproduced in table 4.1.

PROBLEMS IN INTERPRETING EQUATION [4.8].

There are three main problems associated with the equation [4.8] which relates the mutual capacitance between two conductors with the potential difference between the plates and the charge stored. The problems are:

(1) According to [4.8], the capacitance between two plates at the same potential should be infinite.

The above is not true. There is no net flux between the two conductors at the same potential, but their mutual capacitance is finite. This is because on charged bodies charge can be polarised creating areas of negative charge on a positively charged body and vice versa.

(2) Looking at the equation [4.8] one is tempted to say that C depends on potentials on the plates. This also is not true, C must be independent of Q and V. However, as seen from equation [4.10] it depends on the material between the plates, their separation and dimension.

(3) This equation is applicable only when the field between the plates is uniform and there is no fringing of field lines.

Table 4.1: In-Plant Electrostatic Survey Results.

	Average Reading (V)
Person walking across linoleum floor	5000
Person walking across carpet	15,000
Person working at bench	800
Ceramic DIPs in plain plastic tube	700
Ceramic DIPs in plastic set-up trays	4000
Ceramic DIPs in Styrofoam	5000
Circuit packs as bubble plastic cover removed	20,000
Circuit packs as packed foam box	11,000
Circuit packs (packaged) as returned for repair	6000

Problem: A parallel-plate capacitor has plates of area $4m^2$. The moveable plates are immersed in a liquid for which $\epsilon = 4$. A potential difference of 4000 V is maintained between the plates, calculate capacitance, charge per plate, surface charge density, field strength and stored energy in Joules and watt-hours when the separation between the plates is:

(i) 1 cm

(ii) 2 cms

(iii) 4 cms

(iv) 10 cms

Solution:

$$\epsilon_o = 8.854 \times 10^{-12} \text{ F/m}$$

using equation [4.10]

(1) Capacitance, $C = \dfrac{\epsilon \epsilon_o A}{D}$

$$= 4 \times 8.854 \times 10^{-12} \frac{4}{1 \times 10^{-2}}$$

$$= \frac{1.41664 \times 10^{-12}}{1 \times 10^{-2}} = 1.42 \times 10^{-8} \text{ F}$$

Charge $Q = CV = 1.42 \times 10^{-8} \times 4 \times 10^{3}$

$$= 5.66 \times 10^{-5} \text{ Coulomb}$$

Surface charge density $\sigma_s = \dfrac{Q}{A} = \dfrac{5.66 \times 10^{-5}}{4} = 1.4166 \times 10^{-5} \dfrac{\text{Coulomb}}{m^2}$

Field strength $E = V/D = \dfrac{4 \times 10^{3}}{1 \times 10^{-2}} = 4 \times 10^{5}$ v/m

or $$E = \frac{\sigma_s}{\epsilon\epsilon_o} = \frac{1.4166 \times 10^{-5}}{4 \times 8.854 \times 10^{-12}}$$

$$= 4.0 \times 10^{5} \quad \text{v/m}$$

Energy in Joule, $$\frac{CV^2}{2} = \frac{1}{2} \times 1.42 \times 10^{-8} \times (4000)^2$$

$$= 0.1136 \text{ J}$$

1 watt-second = 1 joule

$\therefore$ 1 Watt-Hour = (60 x 60) J

Similary for D = 2, 4 and 10 cms the values can be calculated. The values are given in table 4.2.

Table 4.2

$V = 4 \times 10^3$ volts

D	C	Q	σ_s	E		Energy
meter	Farad	Coulomb	Coulomb/m^2	V/m	Joule	Walt-Hour
1×10^{-2}	1.42×10^{-8}	5.66×10^{-5}	1.42×10^{-5}	4×10^5	0.1136	3.16×10^{-5}
2×10^{-2}	7.08×10^{-9}	2.8×10^{-5}	7.08×10^{-6}	2×10^5	0.0566	1.57×10^{-5}
4×10^{-2}	3.54×10^{-9}	1.42×10^{-5}	3.54×10^{-6}	1×10^5	0.0283	7.86×10^{-6}
10×10^{-2}	1.42×10^{-9}	5.67×10^{-6}	1.42×10^{-6}	4×10^4	0.0114	3.15×10^{-6}

CHARGE AND DISCHARGE OF A CAPACITOR

An ideal capacitor does not have a resistive part associated with it and the dielectric medium is treated as lossless. In this situation immediately upon connecting a d.c. voltage source the capacitor attains its full charge (Q = CV) and the current remain zero. The charging mechanism of a capacitor is fairly complex. All practical capacitor have a resistive component as shown in Fig. 4.6.

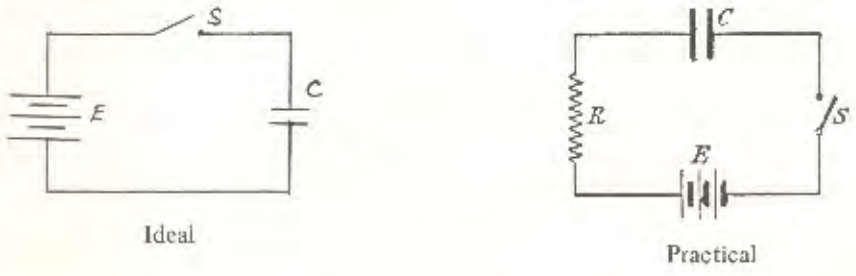


Fig. 4.6 – Practical and Ideal Capacitor Circuit

The equations governing the charging process of the capacitor are [4.8], [4.16] and [4.17]

$$i = \frac{E}{R} \text{ Exp } (-t/CR) \qquad [4.16]$$

$$V_c = E [\ 1 - \text{Exp } (-t/CR)\ ] \qquad [4.17]$$

or $Q_c = EC\ [1 - Exp\ (-t/CR)]$ [4.18]

Since $Q_c = C V_c$

The product of RC is known as the time constant and is measured in second as shown below:

$$RC = \frac{\text{Volt}}{\text{Current}} \times \frac{\text{Charge}}{\text{Volt}}$$

$$= \frac{\text{Volt}}{\text{Charge/Second}} \times \frac{\text{Charge}}{\text{Volt}}$$

$$= \frac{\text{Volts x Second}}{\text{Charge}} \times \frac{\text{Charge}}{\text{Volt}} = \text{Second}$$

Alternatively

$$RC = \text{ohm} \times \text{farad}$$

$$= \frac{\text{volt}}{\text{current}} \times \frac{(\text{charge})^2}{\text{Joule}}$$

$$= \frac{\text{Joule/Coulomb}}{\text{Coulomb/Sec}} \times \frac{(\text{Coulomb})^2}{\text{Joule}}$$

$$= \frac{\text{Joule–Second}}{\text{Coulomb}^2} \times \frac{\text{Coulomb}^2}{\text{Joule}}$$

$$= \text{Second}$$

Because $C = \text{Coulomb / Volt}$

$$= \text{Coulomb / (Joule / Coulomb)} = \frac{(\text{Coulomb})^2}{\text{Joule}}$$

Some interesting conclusions can be drawn from equation [4.16], [4.17] and [4.18]. These are shown in Fig. 4.7.

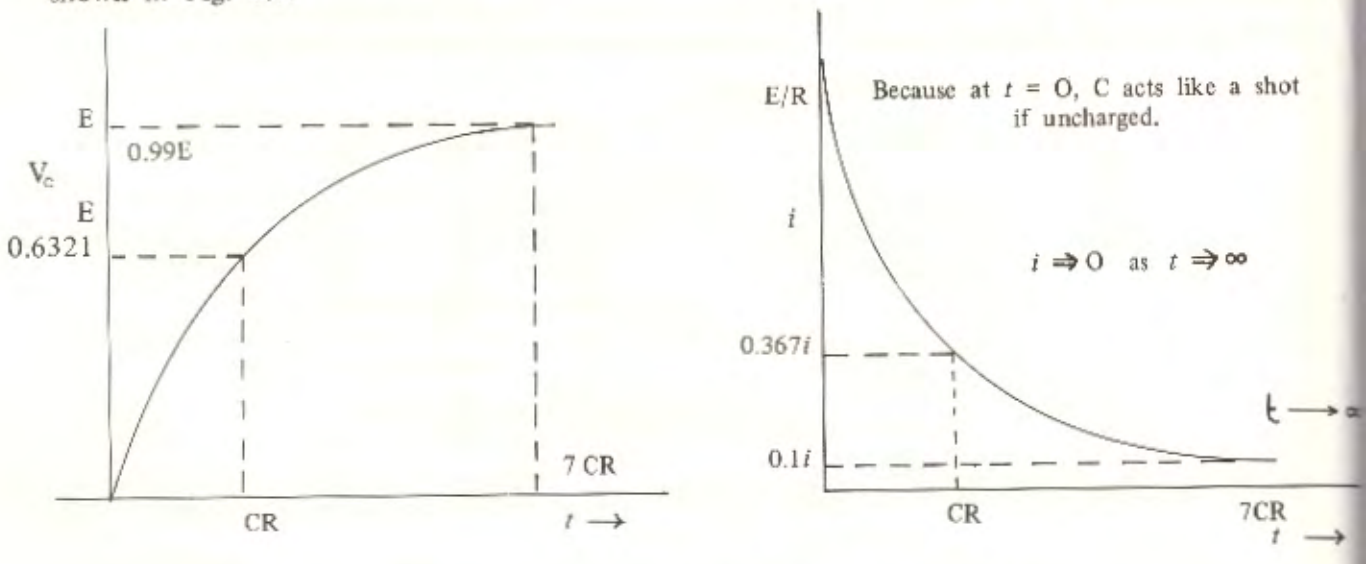


Fig. 4.7 Charging and Discharging Characteristics of a Practical Capacitor.

For a fully charged capacitor the discharging process at the time when the switch S is opened is governed by equations [4.19] and [4.20].

$$i(t) = \frac{E}{R} \text{ Exp } (-t/CR) \qquad [4.19]$$

$$V_c = E \text{ Exp } (-t/CR) \qquad [4.20]$$

The rate at which the capacitor discharges is given by equation [4.21].

$$\frac{dV_c}{dt} = \frac{E}{CR} \text{ Exp } (-t/CR) \qquad [4.21]$$

at $t = O$,

$$-\frac{dVc}{dt} = E/CR$$

It can be concluded that in one time constant ($t = CR$) the voltage would fall to 0.368E.

It must now be clear that the two most important components involved in storing the electrostatic charge and dispensing it away are the capacitance and resistance. This capacitance can appear in an industrial environment in a number of situation including human body, furniture, electrical wiring and so on. The resistance also manifests itself in many ways. To provide adequate protection against ESD damage it is important to know the factors which affect the RC values. The concepts developed here would assist us later in understanding the models of failure modes and mechanisms responsible for ESD induced failures.

5. MODELS FOR ESD INDUCED FAILURES

It is now generally accepted that even with severe protection measures ESD can cause 39 to 48% of the IC rejects. The notion that only MOS devices are ESD sensitive is also disappearing. In fact any electronic component using a semiconducting material as the base can be damaged by ESD. The economic considerations of ESD clearly demands that ESD must be controlled and to initiate a viable programme one must evaluate the level of protection required. The situation is like obtaining an acceptable and desirable insurance policy. Hence for an effective ESD control programme the identification of ESDS[12] (electrostatic Discharge Sensitivity) items is the first and the basic step. As discussed earlier ESD can cause both total failure and degradation of electrical characterics of integrated circuits. The knowledge of ESD induced failure mechanisms and models are essential in designing devices which are more resistant to ESD and also in reducing the failure rate of ESD sensitive devices. This reduction can be achieved virtually at any stage where ESDS items are handled. Unfortunately more human involvement in dealing with ESDS devices means more failure.

ESD induced failures of integrated circuits can be traced to be due to either of the three known models. Generally only one of these mechanisms is involved in the demise of ESDS component, however, in an eventual failure one mechanism may lead to another. The most common failures are due to thermal breakdown, dielectric breakdown, and metalisation melt. These three models are:

(1) The human body model

(2) The charged device model

(3) The field-induced model

By far the human body model has received most attention and is widely used in industry to simulate ESD failures. Speakman's[13] charged device model, though very important for understanding the ESD induced failures in transporting and handling, has received very little attention. The field associated with the accumulated static charges is known to damage MOS devices. Unger[11] has reported failures of such devices when inserted in the uniform field of 6000 v/cm. This model too has not received much attention. The ESDS devices susceptible to failures due to induced field can be protected by using conductive electrostatic shield.

Overheating and breakdown are the two main failure mechanisms observed in integrated circuits. Excessive current through small resistive areas create very high power densities (power per unit area) which physically melts the semiconductor material. Such failures are typical of bipolar devices, diodes and film. In MOS devices, the damage is initiated by the breakdown of the oxide layer under the metalisation due to an excessive electric field across the oxide. This is illustrated for a MOSFET[14] in Fig. 5.1.

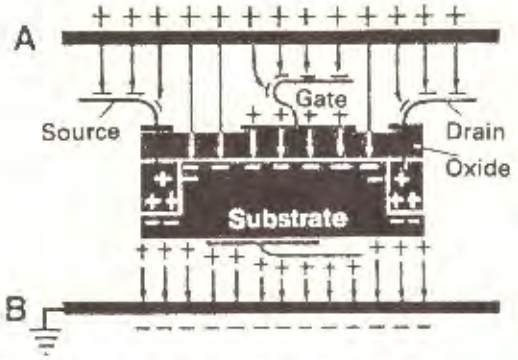


Fig. 5.1 EFFECT OF STATIC FIELD OF MOSFET

ESD Induced Failure of Power MOSFET[15]

One of the biggest operating advantages of the power MOSFET can also be the cause of its demise when it comes to ESD – ultra-high input resistance (typically $> 4 \times 10^9$ ohms). The gate of the power MOSFET may be considered to be a low voltage (± 20V) low leakage capacitor. The capacitor plates are formed primarily by the silicon gate and source metalisation. The capacitor dielectric is the silicon oxide gate insulation.

ESD destruction of the MOSFET occurs when the gate-to-source voltage is high enough to arc across the gate dielectric. This burns a microscopic hole in the gate oxide which permanently destroys the device. Like any capacitor, the gate of a power MOSFET must be supplied with a finite charge to reach a particular voltage. Since larger devices have greater capacitance they require more charge per volt and are therefore less susceptible to ESD than are smaller MOSFETs. Also, immediate failure usually will not occur until the gate-to-source voltage exceeds the rated maximum by two to three times.

A typical ESD destruction site can be seen in Figure 5.2. This was caused by a human body model charged to 700 volts being discharged into the gate of the device. This photo was taken at a magnification of 5,000 with a scanning electron microscope after stripping the surface of the die down to polysilicon. The actual failure site shown in Figure 5.2 is only about 8 microns in diameter. The electrical symptom of ESD failure is a low resistance or a zener effect between gate and source with less than ± 20 volts applied.

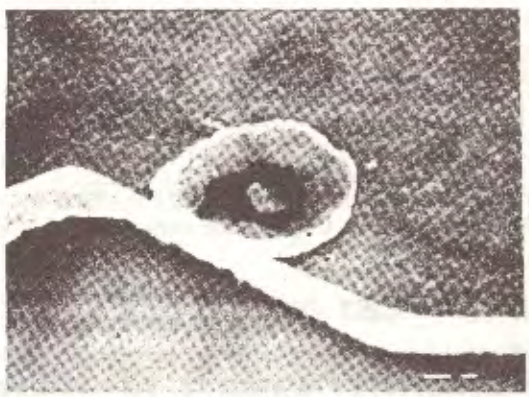


Fig. 5.2 – Typical ESD Failure Site.

The voltages required to induce ESD damage can be 1,000 volts or higher (depending upon chip size). This is due to the fact that the capacitance of the body carrying the charge tends to be much lower than the capacitance of the MOSFET, so that when the charge is transferred, the resulting voltage will be much lower than the original. The graph of Figure 5.3 shows the relationship between chip size and voltage required to induce ESD damage.

Electrostatic fields can also destroy the power MOSFET. The failure mode is ESD but the effect is caused by placing the unprotected gate of the FET in a corona discharge path. Corona discharge is caused by a positively or negatively charged surface discharging into small ionic molecules.

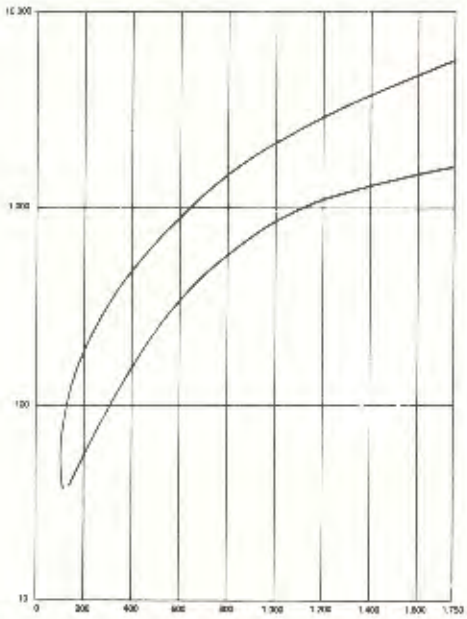
IDENTIFICATION OF ESDS

An effective ESD control programme cannot be implemented unless ESDS of items has been properly identified. The contractors must know the ESDS items and their level of sensitivity. This knowledge is critical for the contractor for design, handling, packaging, training and programme monitoring. Such items must be clearly identified in all documents using standard labels and markings. The document must contain or refer to safe handling procedure.

According to MIL-STD-DOD-HDBK 263 [Electrostatic Discharge Control Handbook For Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)] ESDS items are Categorised in three classes as below:

- Class 1 : Sensitivity range 0 to $\leq$ 1000 Volts
- Class 2 : Sensitivity range $>$ 1000 to $\leq$ 4000 Volts
- Class 3 : Sensitivity range $>$ 4000 to $\leq$ 15,000 Volts

The details of the ESDS parts which have been classified as above as contained in DOD-HDBK 263 are given in Table 5.1.



ESD VOLTAGE Fig. 5.3 – Capacitance versus ESD Failure Voltage.

TABLE 5.1 – LIST OF ESDS parts by part type

CLASS 1: SENSITIVITY RANGE 0 TO _ 1000 VOLTS
• Metal Oxide Semiconductor (MOS) devices including C, D, N, P, V and other MOS technology without protective circuitry, or protective circuitry having Class 1 sensitivity.
• Surface Acoustic Wave (SAW) devices.
• Operational Amplifiers (OP AMP) with unprotected MOS capacitors.
• Junction Field Effect Transistors (JFETs) (Ref.: Similarity to MIL-STD-701: Junction field effect, transistors and junction field effect transistors, dual unitized).
• Silicon Controlled Rectifiers (SCRs) with Io $<$ 0.175 amperes at 100° Celsius (°C) ambient temperature (Ref.: Similiarity to MIL-STD-701: Thyristors (silicon controlled rectifiers)).
• Precision Voltage Regulator Microcircuits: Line or Load Voltage Regulation $<$ 0.5 percent.
• Microwave and Ultra-High Frequency Semiconductors and Microcircuits: Frequency $>$ 1 gigahertz.
• Thin Film Resistors (Type RN) with tolerance of $\ll$ 0.1 percent; power $>$ 0.05 watt.
• Thin Film Resistors (Type RN) with tolerance of $>$ 0.1 percent; power $\leq$ 0.05 watt.
• Large Scale Integrated (LSI) Microcircuits including microprocessors and memories without protective circuitry, or protective circuitry having Class 1 sensitivity (Note: LSI devices usually have two to three layers of circuitry with metallization crossovers and small geometry active elements).
• Hybrids utilizing Class 1 parts.

CLASS 2: SENSITIVITY RANGE 1000 TO _ 4000 VOLTS

- MOS devices or devices containing MOS constituents including C, D, N, P, V, or other MOS technology with protective circuitry having Class 2 sensitivity.
- Schottky diodes (Ref.: Similiarity to MIL-STD-701: Silicon switching diodes (listed in order of increasing trr)).
- Precision Resistor Networks (Type RZ).
- High Speed Emitter Coupled Logic (ECL) Microcircuits with propagation delay $\leq$ 1 nanosecond.
- Transistor-Transistor Logic (TTL) Microcircuits (Schottky, low power, high speed, and standard).
- Operational Amplifiers (OP AMP) with MOS capacitors with protective circuitry having Class 2 sensitivity.
- LSI with input protection having Class 2 sensitivity.
- Hybrids utilizing Class 2 parts.

CLASS 3: SENSITIVITY RANGE 4000 TO _ 15,000 VOLTS

- Lower Power Chopper Resistors (Ref.: Similarity to MIL-STD-701: Silicon Low Power Chopper Transistors).
- Resistor Chips.
- Small Signal Diodes with power $\ll$ 1 watt excluding Zeners (Ref.: Similarity to MIL-STD-701: Silicon Switching Diodes (listed in order of increasing trr)).
- General Purpose Silicon Rectifier Diodes and Fast Recovery Diodes (Ref.: Similarity to MIL-STD-701: Silicon Axial Lead Power Rectifiers, Silicon Power Diodes (listed in order of maximum DC output current), Fast Recovery Diodes (listed in order of trr)).
- Low Power Silicon Transistors with power $\ll$ 5 watts at 25°C (Ref.: Similarity to MIL-STD-701: Silicon Switching Diodes (listed in order of increasing trr), Thyristors (bi-directional triodes), Silicon PNP Low-Power Transistors (Pc $\ll$ 5 watts @ T_A = 25° C), Silicon RF Transistors).
- All other Microcircuits not included in Class 1 or Class 2.
- Piezoelectric Crystals.
- Hybrids utilizing Class 3 parts.

However, DOD-HDBK-1686 only refers to two classes as above. These sensitivities are based on human body model simulated by taking the values of body capacitance and resistance as 100 pF and 1.5 K ohms respectively. These values will not apply if the test circuit has different values.

TEST SET UP TO IDENTIFY ESDS PARTS

The test circuit specified for testing the sensitivity of ESDS parts in accordance with MIL-M-38510 (Military Specification, Microcircuits, General Specifications for). This test circuit does not take care of the worst situation represented by R and C values. A study performed on human body capacitance indicated that approximately 80%[16] of the population tested had a capacitance of 100 pF or less. The test setup is shown in Fig. 5.4. Reported susceptibility ranges of various devices exposed to static discharge are given in Table 5.2 and Fig. 5.5

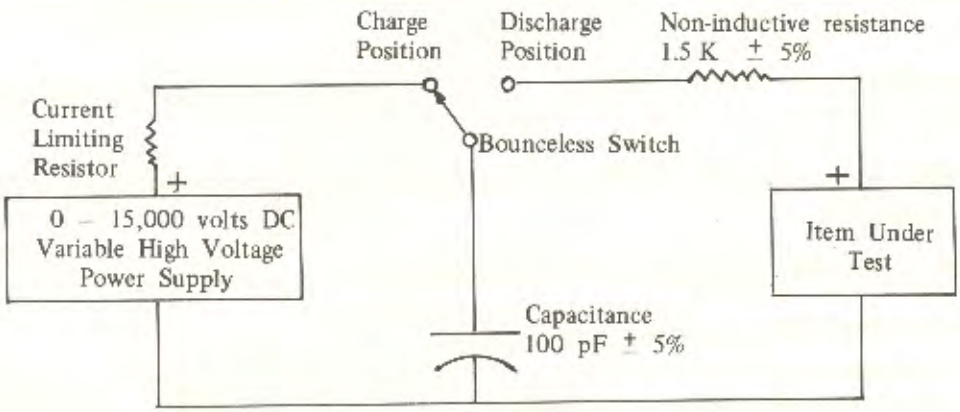


Figure 5.4 – ESD test circuit

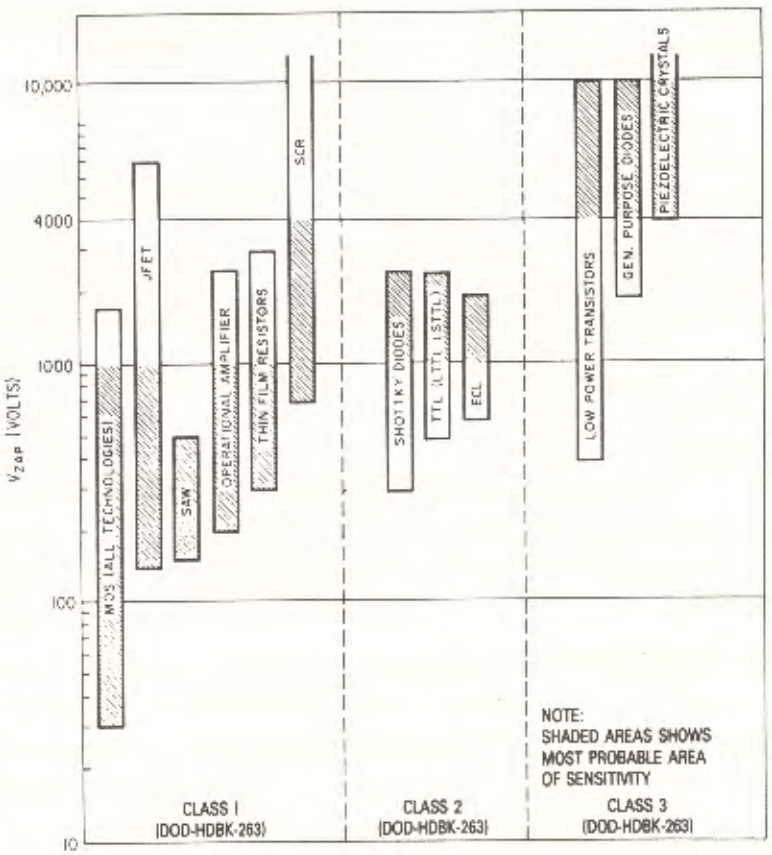


Fig. 5.5 – Known and most probable (shaded) sensitivities of different parts.

TABLE 5.2
REPORTED SUSCEPTIBILITY
RANGES OF VARIOUS DEVICES
EXPOSED TO STATIC DISCHARGE

Device Type	Range of Static Discharge Susceptibility (Volts)
VMOS	30-1800
MOSFET	100-200
GaAsFET	100-300
EPROM	100
JFET	140-7000
SAW	150-500
OP-AMP	190-2500
CMOS	250-3000
Schottky Diodes	300-2500
Film Resistors (Thick, Thin)	300-3000
Bipolar Transistors	380-7000
ECL	500-1500
SCR	680-1000
Schottky TTL	1000-2500

THE HUMAN MODEL

The discharge of electrostatic voltage from human body to the device has been simulated by two equivalent circuits shown in Fig. 5.6. In the model C_b, R_b and L_b are:

Fig. 5.6 – The Equivalent Circuit of The Human Model

C_b Capacitance of human body to ground. Widely accepted minimum and maximum values of C_b are 50 pF and 300 pF. 100 pF is taken as the typical value.

R_b Resistance of the human body. Widely accepted values of R_b are 1 K ohms to 30 K ohms. 1.5 K ohm is taken as the typical value.

L_b Self-inductance of the loop formed by the body, its arm, the machine and the ground return. Widely accepted minimum and values of L_b are 0.3 μH to 1.5 μH. 0.7 μH is taken as the typical value.

The nature of the ESD waveform[17] characterising the discharge process is shown in Fig. 5.7. The static discharge pulse is characterised by the peak value of the current, the rise time of the current pulse, measured between the 10% and 90% (approximately corresponding to the rise time of the triangular pulse) and pulse width at 50% amplitude. The typical values are shown in Fig. 5.7.

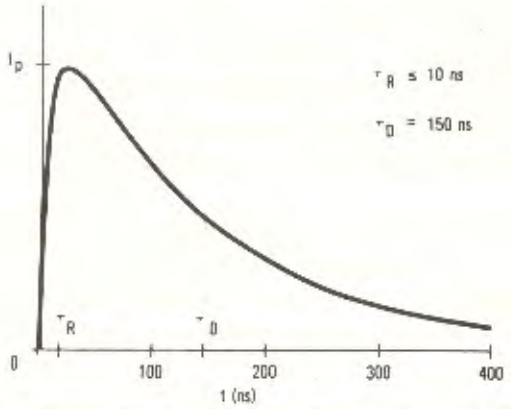


Fig. 5.7 – Static Discharge Short Circuit Current Waveform

One of the main problems in using the human body model is the choice of C_b, R_b and L_b. The rise time of the discharge would be infinitely small if the inductance L_b was absent and C_b simply discharged in a resistive circuit. The rise time Z_R is dictated by the ratio of L_b/R_b and the pulse width is determined by the R_bC_b time constant. The extent of variation in R_b is shown in Fig. 5.8. The variation in human capacitance is due to factors such as variation in the amount and type of clothing and shoes worn by personnel and differances in floor material. The variation in human resistances is due to factors such as the amount of moisture, salt and oil at skin surface, skin contact area and pressure. The capacitance value in conjunction with R_b determines the peak current value of the discharge pulse shown in Fig. 5.7 and C_b value can change by an order of magnitude within the working area. These values have been be estimated by Yenni[18] and are given in Table 5.3. Keller[19] has provided an empirical formula for calculating the human body capacitance from body size parameters. The human body capacitance C_b is divided into two major parts:

(i) The parallel-plate capacitance of the soles of the feet to ground.

(ii) The capacitance of the body bulk to ground.

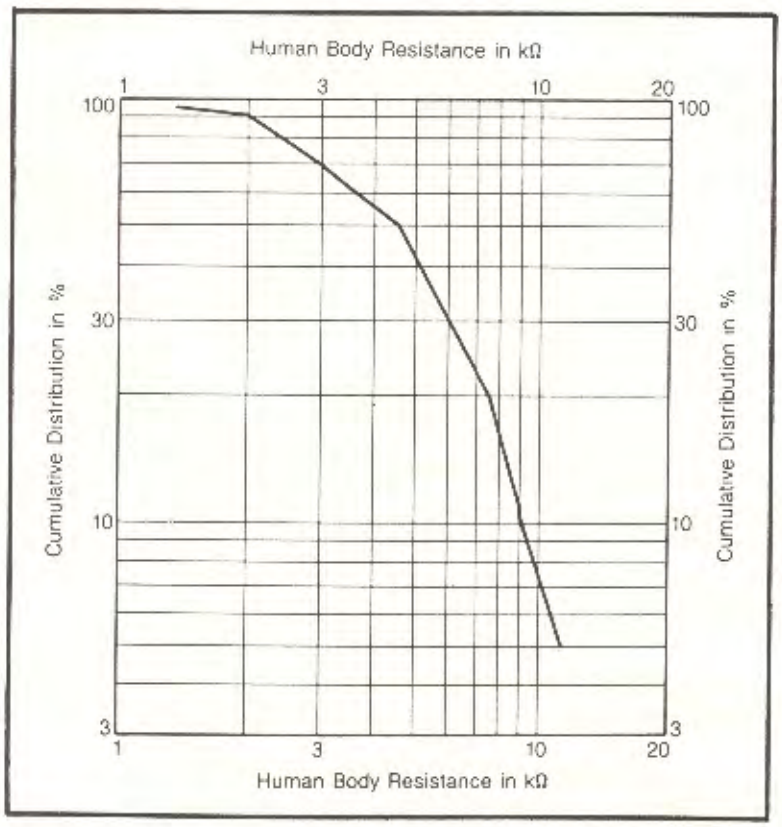


Fig. 5.8 – Distribution of human body resistances: probability (P) that R will be exceeded.

Table 5.3 – Capacitance Changes in Personnel in a Work Area.

Description of Movement	*% Change in Capacitance Due to Movement*		
	Initial Capacitance	*Final Capacitance*	*% Change*
Person seated, raising one foot	192	163	15% decrease
Person seated, picking up both feet, and placing them on the foot rest	192	129	33% decrease
Person seated, leaning forward in chair (desk-type chair with back)	192	184	4% decrease
Standing person, raising one foot	167	141	16% decrease
Seated person, standing up	192	167	13% decrease

In an attempt to resolve the problem Madzy [120] performed a rather unique experiment in which he selected six brave people who charged themselves to a high-voltage power supply and discharged on a grounded 1 ohm shunt. The RC experiment as reported by Madzy is shown in Fig. 5.9. The charging path included a 100 M ohm resistor to limit the current. This experiment was done to find out the values of C_b and R_b. The waveshape of the discharge current was recorded and the capacitance of the body was measured with respect to ground. Knowing the R_bC_b time constant and the body capacitance C_b the body resistance R_b can then be calculated. The values of R_b and C_b obtained by Madzy are given in Table 5.4. The body capacitance ranged from 140 pF to 180 pF except for the person No. 6 (a female wearing thick sole shoes). Some of the drawbacks of this experiment were:

- Detailed information about the experimental objects was not reported. The size, race, sex, nature of the skin and age etc ought to have been reported.
- It is known that C_b and R_b values can change with ambient conditions and as such temperature, relative humidity and other conditions of the environment should have been reported.
- Surrounding is known to affect these values and as such in a daring experiment of this nature these details should have been given.

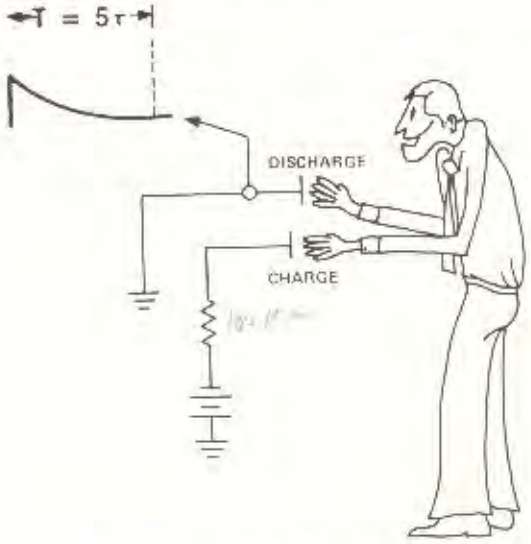


Fig. 5.9 – RC Experiment–Non conductive shoes/surface.

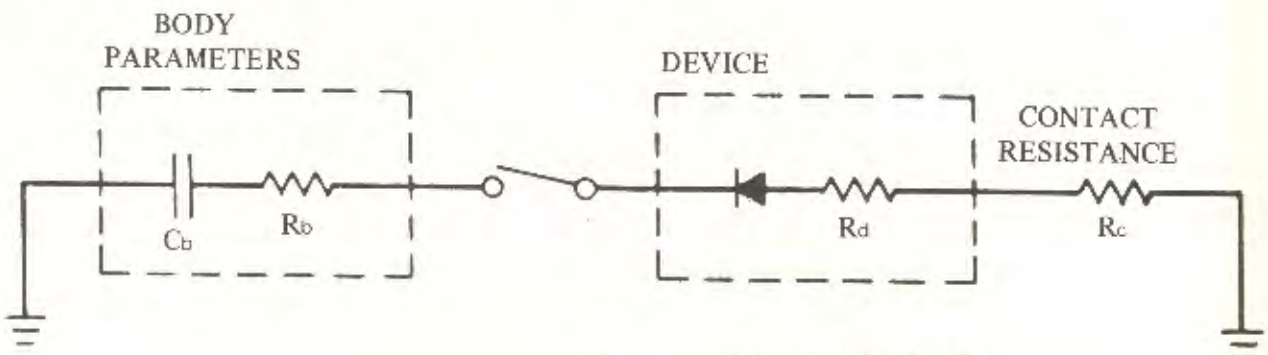
Table 5.4: C_b/R_b Experimental Results

Person #	C_b (pF)	τ (μ sec)	Rb (KΩ)
1	140	.30	2.1
2	145	.30	2.0
3	140	.30	2.1
4	170	.40	2.3
5	180	.35	1.9
6	80	.15	2.4

It is therefore concluded that to verify the reported results would be difficult. However, the same experiment can be performed in a controlled experimental environment to observe the effect of above factors.

To show the effect C_b and R_b values in determining the susceptibility of FET devices Madzy subjected six FETs to a discharging circuit of different values of C_b, R_b and V_p (peak voltage). The equivalent circuit of the discharge circuit is shown in Fig. 5.10 and the values used in Table 5.5. It is obvious from this table that C_b and R_b values influence the damage level (V_p) by a large amount ($\gtrsim$10 time ratio). Madzy has also shown that the damage level (V_p) is a function of pulse width and this level is found to decrease with increasing pulse width.

Most of the ESD simulator are based on human body model with their equivalent circuit as shown in Fig. 5.6(a) and it is no surprise that Madzy also did not include L_b in his experimental circuit. The self inductance of the body was not included because the study was mainly aimed at determining the destructive effect of ESD when handling devices, modules and assemblies. In such situations the pulse width is the main concern and not the rise time which is determined by L_b/R_b. The nature of the reported ESD waveform and its exact shape represented by the actual values of C_b and R_b can vary a great deal. Tucker[21], King[22, 23] and Byrne[24] and many other researchers have reported some interesting waveforms. A complete equivalent circuit representing the human body model and the device is shown in Fig. 5.10.



C_b – BODY CAPACITANCE
R_b – BODY RESISTANCE
R_d – DEVICE RESISTANCE
R_c – RESISTANCE TO GROUND

C_b = 100 to 200PF
R_b = 500 to 2000 ohms

Fig. 5.10 – The Human Body Model of ESD

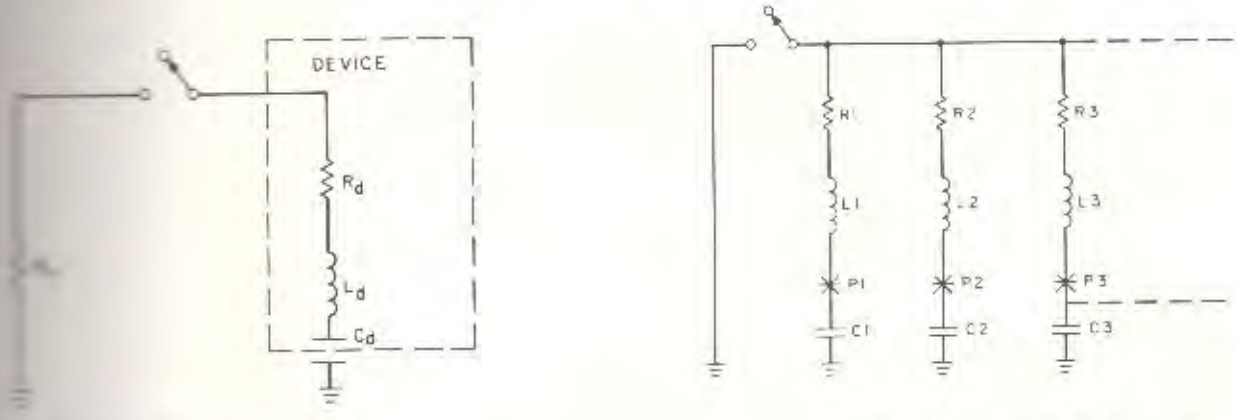
Table 5.5: Damage Levels vs. Varying RC

Test No.	C_b (pF)	R_b (k Ω)	Vp (kV)
1	10	0.5	1.70
2	10	2.0	3.00
3	150	0.5	0.50
4	150	2.0	1.10
5	470	0.5	0.35
6	470	2.0	0.85

CHARGED DEVICE MODEL

A semiconductor device, particularly plastic moulded type, can store significant electrostatic charge on its lead frame and quickly discharge to an effective ground through a low impedance path. In this the charges reside on the metal parts of the die and package. The charges can flow through the die and damage the junction, dielectric, and other component that form the part of the earth circuit in the discharge path. The electrostatic energy stored in the charged device depends on its capacitance which is found to be a function of its orientation with respect to ground.

The electrical equivalent circuits for MOS and bipolar devices are slightly different as shown in Fig. 5.11.



(a) Model For Bipolar Device (b) Model For MOS Structure

Fig. 5.11 – Charge Device Model For Bipolar and MOS Structure

The model consists of resistance, inductance and capacitance in the discharge path. For the bipolar device it is represented by the device resistance R_d, device inductance L_d and device capacitance C_d and some contact resistance R_c (low resistance) through which the charged devices shed the stored charge to the ground. The charged device model for MOS as shown in Fig. 5.11 (b) consists of a number of discharge paths in which R_i L_i and C_i are the resistance, inductance and capacitance of the i^{th} discharge path, respectively, and P_i and P_{i+1} are the points between which the electrostatic potential is calculated as a function of time. Thus in a MOS device there can be a number of discharge paths and the most sensitive path will be affected first, when one pin is grounded, each path responds with its own characteristics depending upon the ratio L_i/R_i and the time constant R_iC_i. Two adjacent paths with significant differences in their discharge characteristics, potentials exceeding the dielectric breakdown of the insulation, mainly SiO_2, between paths can result in the device failure. The voltage at which this breakdown can occur is the function of oxide thickness, which is being consistenatly reduced to obtain fast devices. Typical gate-oxide cross section for a range of technologies[25, 26] is shown in Fig. 5.12. The dielectric breakdown[27] strength of SiO_2 is approximately (6–9) x 10^6 V/cm. Thus a 250 Å gate oxide will not sustain voltage in excess of 20V. The most vulnerable portion of the metal gate device is shown in Fig. 5.13.

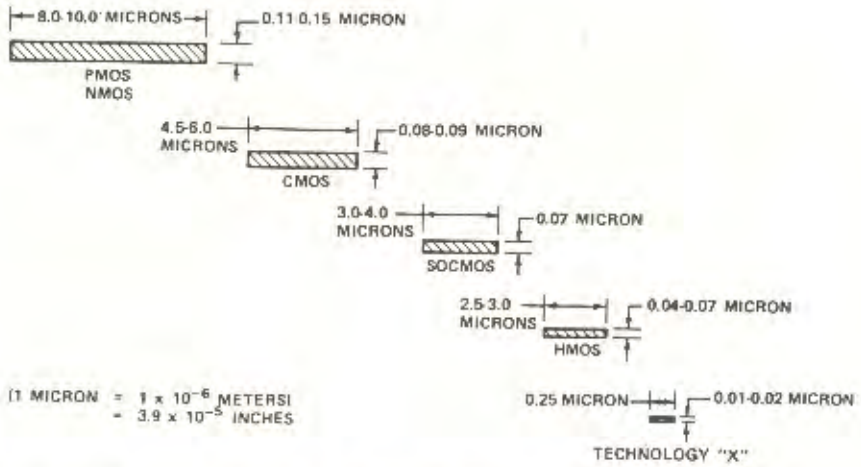
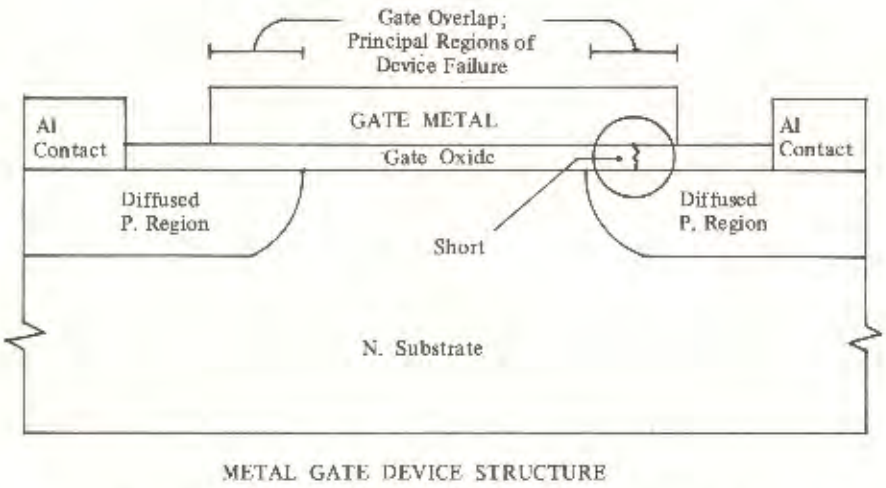


Fig. 5.12 – Typical Gate Oxide Cross Sections – Reduction to Improve Circuit Density and Response Time Constraints



METAL GATE DEVICE STRUCTURE

Figure 13 – Typical metal gate device structure showing short circuit caused by ESD.

EFFECT OF DEVICE ORIENTATION ON ITS CAPACITANCE

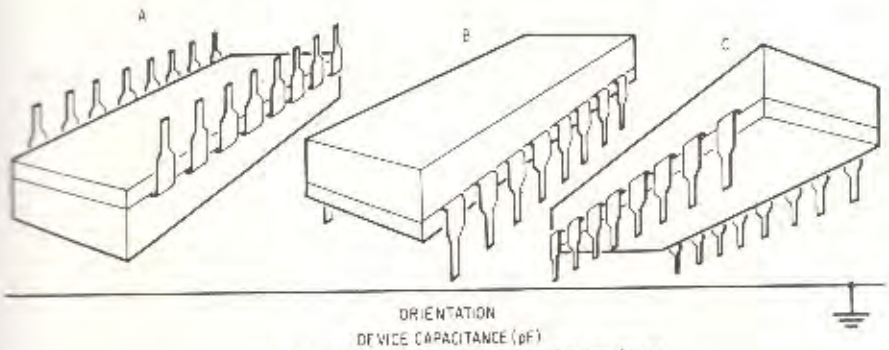
The effect of orientation on device capacitance for a number of devices in DIP packages was studied by Unger[11]. The measurement was done with the device resting on a ground plane. The orientation and the values obtained by Unger are shown in Fig. 5.14. A device close to ground plane will have a higher capacitance than the same device would have at some distance from the ground plane. In these situations the device, be it a DIP, hybrid or other package, acts as the plate of a capacitor, storing a charge Q. Depending upon the orientation the ratio of maximum to minimum device capacitance can be as high as 18. This means the energy stored ($\frac{1}{2}$ CV^2) can be controlled, and reduced if the devices can be kept in orientation as marked C.

Madzy[28] conducted ESDS tests on MOSFETS under various orientation as shown in Fig. 5.15. The tests were performed using human body ESD simulator with C_b and R_b values of 150 pF and 2 K ohm respectively. In case 1, 2 and 3 there were no failures with positive polarity voltages up to 5 kV applied to the case or a pin. In case 1, 2, 3, 4 and 6 there were no failures with negative polarity voltages up to 5 kV. However in case 4 and 6 failures were observed with a positive voltage in the range of 1,200 to 2,000 V and 1,200 to 1,400 V respectively. The orientation represented by case 5 resulted in failures with negative voltage of 1,800 V.

In an other experiment reported by Bossard[29] et. al., 2×10^{-9} coulombs were put on a 16-pin DIP to determine the magnitude of the charge transferred to integrated circuit packages during handling. This charge can be readily attained by triboelectric charging of device lead frame in plastic shipping tubes during handling. The device under test was discharged to ground through a 1 ohm resistor and 1 GHz scope was used to record the transient current pulse. The set-up used is

above in Fig. 5.16. The discharge pulse rise time was typically 0.5 x 10^{-9} second and the duration of the entire event was several nano seconds. The peak current observed by Bossard et. al. was in excess of 14A, with average power dissipated greater than 1 kW and average power density higher than 10^{9} w/cm^2. Bossard et. al. concluded from this experiment that devices charged as above can be safely discharged on a work surface with sheet resistance of 10^5 ohm/□ or greater. A discrete 10^{9} ohm resistor grounding a metallic table top is found to be ineffective in reducing the power densities because the capacitance of the table top acts as an effective ground.

The values of the calculated current and energy as a function of time for the device discharge model are shown in Fig. 5.17. The photograph of an ESD pulse from a 16-pin device, with parameters similar to one shown in Fig. 5.17, and charged to 500 V, is shown in Fig. 5.18. Also shown in photograph (Fig. 5.18) are the discharge traces of pins on a MOS device after charging to 200 V, these traces show the variation in discharge period.



ORIENTATION

DEVICE CAPACITANCE (pF)

	16-PIN DIP (PLASTIC)	18-PIN DIP (PLASTIC)	24-PIN DIP (PLASTIC)	24-PIN DIP (CERAMIC SIDE, BRAZED)	40-PIN DIP
A	2.9	3.6	7.1	28	52
B	2.0	2.3	3.9	3.6	6.6
C	1.4	1.6	2.0	2.0	2.8
C_{max}/C_{min}	2.0	2.2	3.5	14	18.6

Fig. 5.14 – Capacitance variation with device orientation.

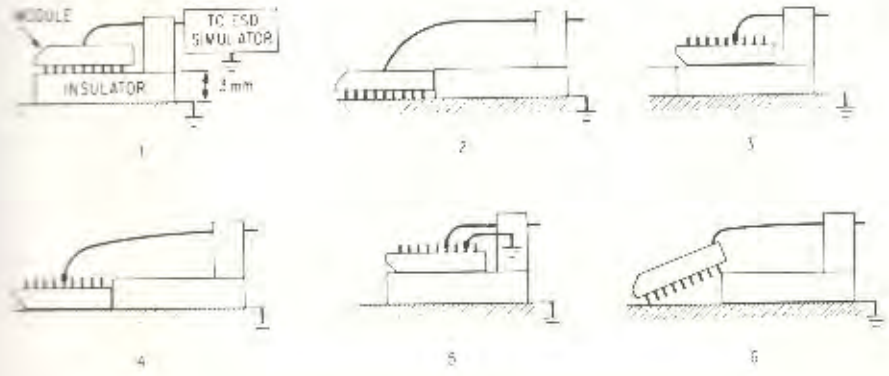


Fig. 5.15 – MOSFET orientations for ESD sensitivity testing.

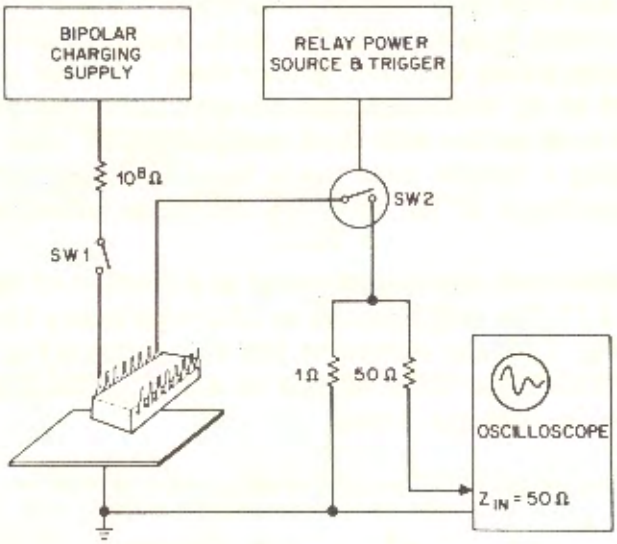


Fig. 5.16 – Schematic of device charge/discharge ESD model test fixture.

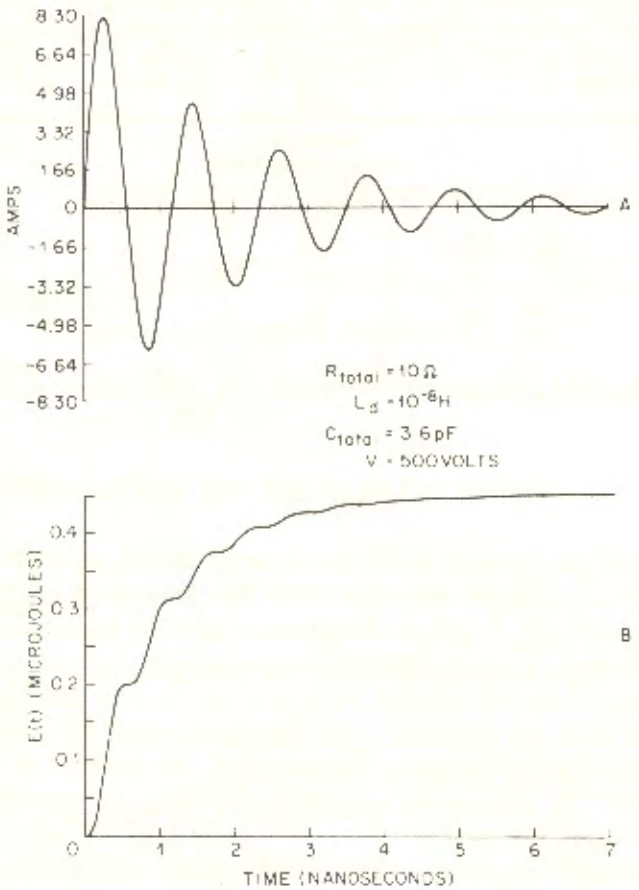


Fig. 5.17 – Calculated current (*A*) and energy (*B*) as a function of time for the device discharge model with conditions noted.

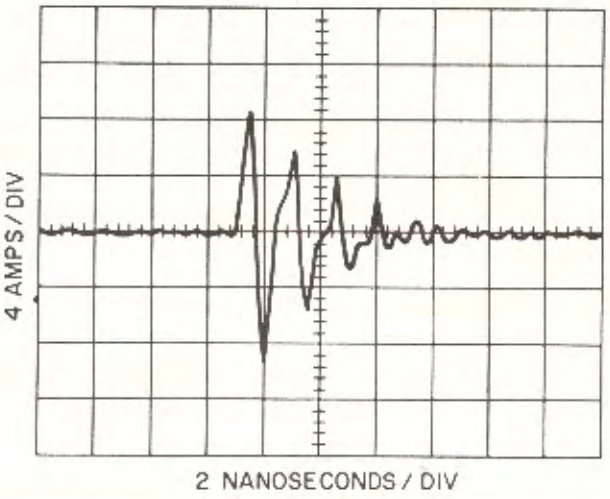


Fig. 5.18(a) – Photograph of an ESD pulse from a 16-pin device with parameters similar to those used in the calculations of Fig. 5.17. The device was charged to 500V (1.8 nC).

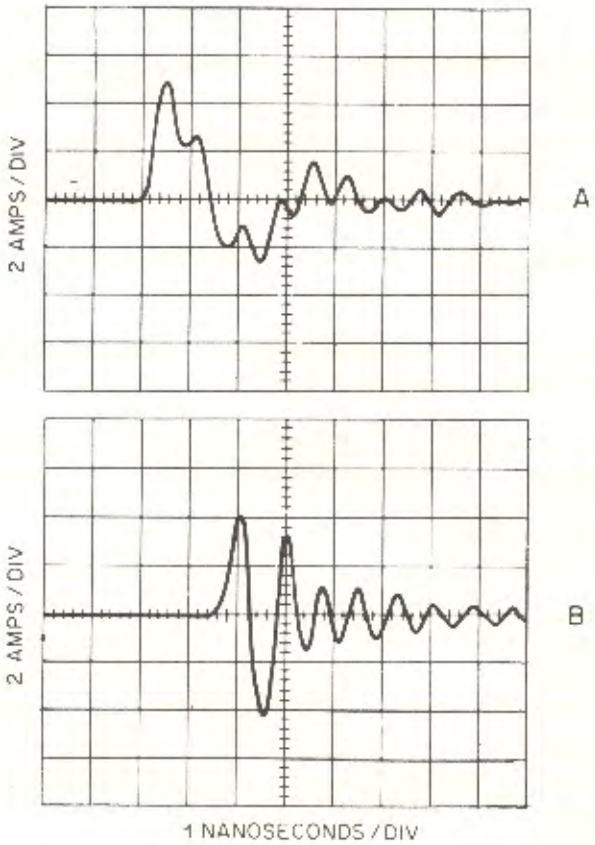


Fig. 5.18(b) – Discharge traces of pins on an MOS device after charging to 200V. The traces show the variation in discharge period.

It can be concluded from the above discussion that the electrostatic charge on a device is a potential source of damage. The grounding of a charged device can produce a discharge pulse that can degrade or destroy a device. The electrostatic energy, sufficient to damage or degrade the device, can be stored on a device by the movement of devices in plastic shipping tubes. Damage can result when the device exits from the tube and is discharged to ground. Device damage can be caused in the following two ways:

- Localised heating in the discharge path.
- Breakdown of an oxide due to differences in path characteristics.

To overcome the problem safely a work surface with a minimum sheet resistance of 10^5 ohm/$\square$ is required. King [30] and Chase [31] have discussed the charged device model in some detail.

THE FIELD - INDUCED MODEL

It has been seen in the earlier section that every charge has its own associated field. The electrostatic field is known to originate at a positive charge and terminate at the negative. A potential gradient exists between a charged object and the ground. A device inserted in a high field can have a potential induced across some oxide areas. Under certain conditions of structure and orientation, the induced field may exceed the dielectric strength of the oxide and create a breakdown. It must be remembered that in this case there is no direct contact made between the charged object and the ground.

Bipolar and MOS structures are differently affected by the induced field, this is because of their difference in capacitive configuration and values. Some of the important points to keep in mind regarding static fields and induced charges are:

- Static fields are invisible, but they exist around all charged materials.
- No physical contact between the charged material and conductor is necessary to induce a charge.
- So long as the field moves near a conductor, or a conductor moves near the field, an induced current will flow in the conductor.
- The amount of current that will flow depends primarily on the strength of the field and the speed of the movement.

ESD SPARK INDUCED FAILURES

The phenomenon is similar to spark seen or heard when a charged person, on a dry sunny day having walked on a synthetic carpet, touches a metallic door handle. A spark is generated when a charged person approaches either an ESD sensitive device or a metallic box. The spark generates a travelling electromagnetic field. This is similar to electrostatic field, except that it has its own motion, magnitude and duration. The spark induced failures could be soft or hard depending upon the values of induced current or voltage in the ESD sensitive items. The spark discharge can travel to ground through many different paths:

- It can jump across the insulated portions.
- It can flow through the equipment frame.
- It can flow along the cables.
- It can flow along the tracks of PCBs
- It can flow along power, signal and ground lines.

The ESD spark induced radiation has both electric and magnetic field as demonstrated by Costache et. al[32] shown in Fig 5.19. Costache et. al. have reported that the radiated field with its sharp peaks affects digital circuits more than the analog circuits and as such new generation of equipment used for processing information are greatly affected. The frequency range of these sparks is well over 100 MHz. When ESD sparks on a metallic object, it begins to radiate like an antenna and results in Electromagnetic Interference (EMI). Fig 5.20, 5.21, and 5.22 show how ESD spark generated electromagnetic fields can affect ESDS items. EMI generated from static discharge can enter the ESDS parts by:

- Conduction
- Capacitive or Inductive Coupling
- Radiation

The elimination of ESD/EMI problems is difficult because of its complex nature. However, the problem can be minimised by following good engineering practices on:

- Grounding
- Bonding
- Wiring
- Shielding
- Using ESD - protective materials.

This Problem can be controlled by controlling the environment by designing systems with immunity to spark radiated transients. Walker's[32] hand book contains a good description on how to minimise ESD/EMI Problems.

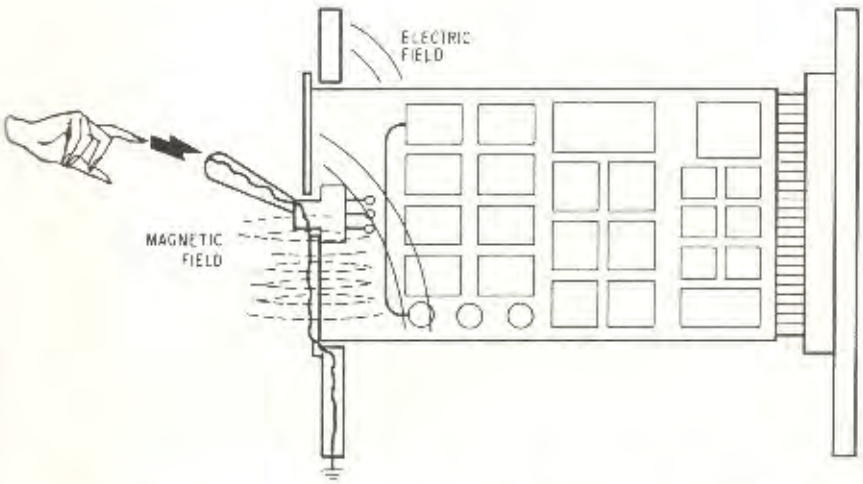


Fig. 5.19 – Electrostatic energy coupling through electric and magnetic fields.

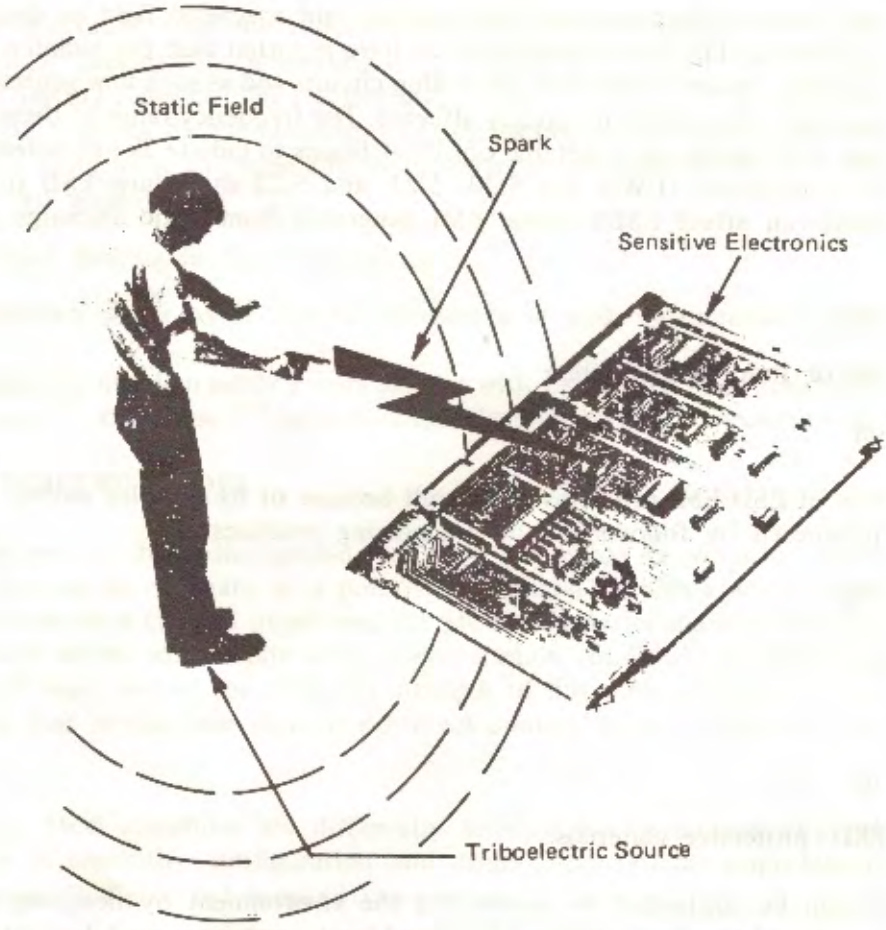


Figure 5.20 – Electromagnetic pulse.

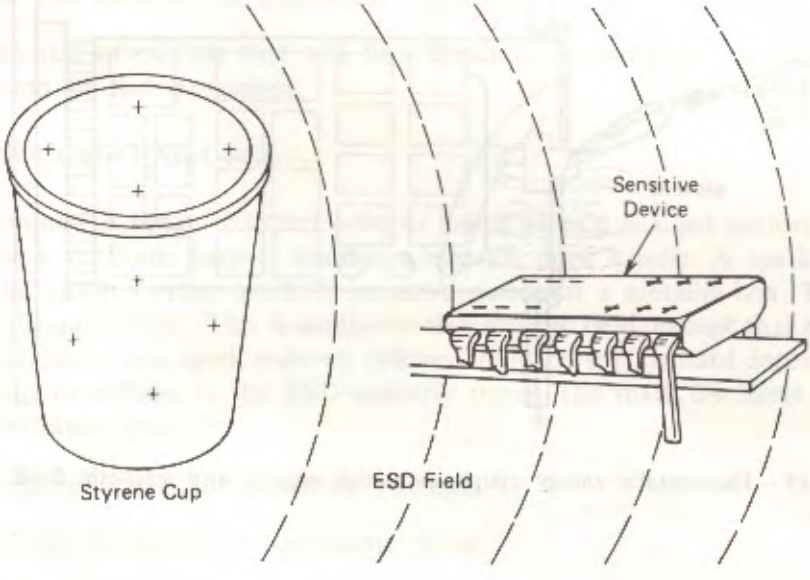


Figure 5.21 – Polarization.

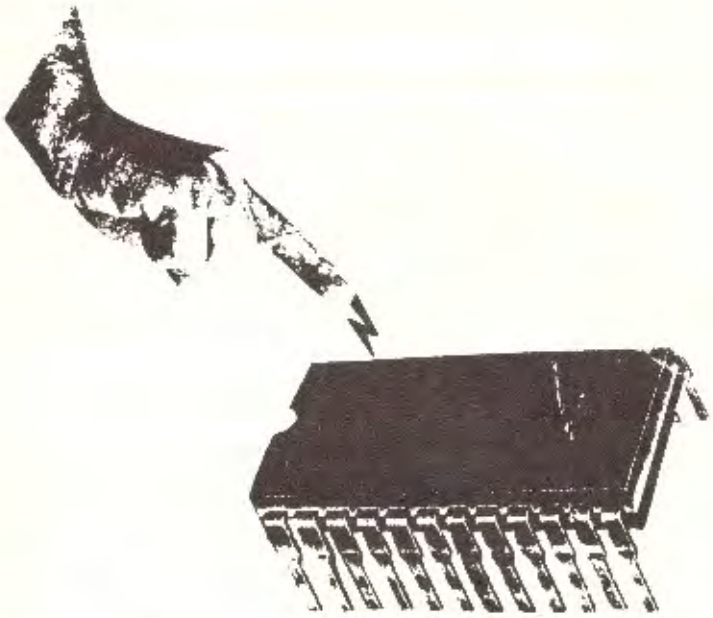


Figure 5.22 (a) – An isolated device exposed to ESD; it retains the charge.

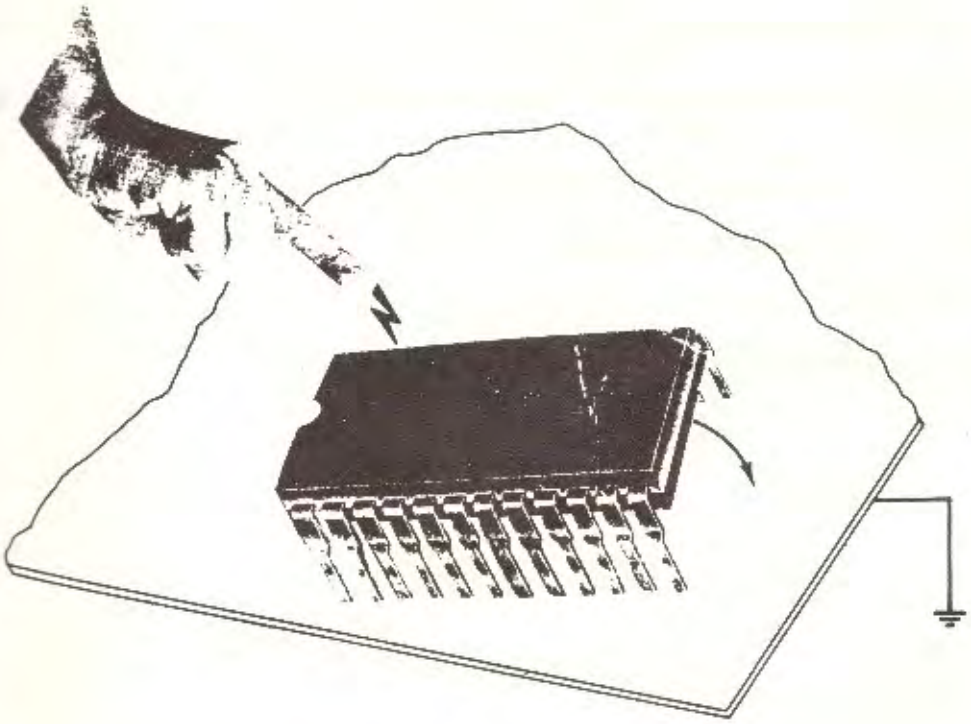


Figure 5.22 (b) – Equivalent Circuit For Wunsch-Bell Model

WUNSCH-BELL MODEL OF ESD INDUCED FAILURES OF BIPOLAR DEVICES

The basic failure mechanism of bipolar devices and metalisation stripes is thermal burn out. Wunsch-Bell[34] proposed a model to determine the threshold voltage which will damage diodes and transistors. The current flowing through device causes heating by raising the local temperature. Wunsch-Bell, model relates the dissipated power density (watts/cm^2) to the thermal characteristics of the semiconductor. This is then related to the local temperature rise to determine the threshold power density responsible for device failure. To achieve a simple solution a one-dimensional model for heat flow was considered when a reverse-polarity pulse was applied to the junction with high reverse breakdown voltage. Power density in this situation is given by equation [5.1]

$$P/A = \sqrt{\pi\ k\ \rho\ C_p}\ [T_m - T_i]\ t^{-0.5} \qquad [5.1]$$

where

P = Power
A = Junction Area
k = Thermal Conductivity
ρ = Density
C_p = Specific Heat
T_m = Failure Temperature (Melting Temperature)
T_i = Initial Temperature
t = Time (Pulse Width).

Assumption Of Wunsch-Bell Model

The prediction of failure levels of ICs using this model depends on the validity of the following assumptions:

(1) Almost all the power is dissipated in the junction.

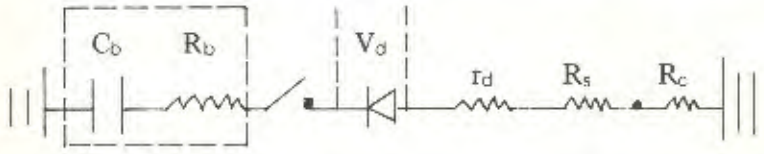
(2) Heat flows only in one direction.

(3) Cross sectional area of the current path is taken to be the junction area.

(4) Average power is dissipated within five time constants.

CALCULATION OF ESD VOLTAGE FOR THE FAILURE OF BIPOLAR DEVICES:

The equivalent circuit used for the calculation is shown in Fig. 5.23



HUMAN BODY

C_b & R_b Body capacitance and resistance.

V_d Voltage drop across the junction (Reverse or Forward depending upon the direction of the current flow).

r_d Dynamic resistance of the junction.

R_s Bulk resistance of the semiconductor.

R_c Contact resistance of the device lead to the ground.

Fig. 5.23 – Equivalent Circuit For Wunsch-Bell Model.

Discharge current through the device is given by equation [5.2]

$$i(t) = I_p \text{ Exp } (-t/\tau) \qquad [5.2]$$

and

$$I_p = \frac{V_{ESD} - V_d}{R_b + r_d + R_s + R_c} \qquad [5.3]$$

where

I_p = Peak Current

τ = Time constant of the discharge path

$= (R_b + r_d + R_s + R_c)\, C_b$

The total power dissipated at or near the junction is given by P(t):

$$P(t) = V_d\, i(t) + R_s\, i^2(t)$$

$$= V_d\, I_p\, Exp\ (-t/\tau) + R_s\, I_p^2\, Exp\ (-2t/\tau)$$

$\therefore$ From assumption No. 4:–

$\therefore$

$$P_{av} = \frac{1}{5\tau}\left[\int_0^{5\tau} P(t)\, dt\right]$$

$$= \frac{1}{5\tau}\left[\int_0^{5\tau} V_d\, I_p\, Exp\ (-t/\tau)\, dt + \int_0^{5\tau} R_s\, I_p^2\, Exp\ (-2t/\tau).\, dt\right]$$

$$= \frac{I_p}{5\tau}\left[V_d \int_0^{5\tau} Exp\ (-t/\tau)\, dt + \int_0^{5\tau} R_s\, I_p\, Exp\ (2t/\tau)\, dt\right]$$

Let $t/\tau = x$ $\quad\therefore\quad dt = \tau\, dx$

When $t = 5\tau$ $\quad x = 5$

$t = 0$ $\quad x = 0$

$\therefore$

$$P_{av} = \frac{I_p}{5\tau}\left[V_d \int_0^{5\tau} Exp\ (-x)\, dx + R_s\, I_p \int_0^{5\tau} Exp\ (-2x)\, dx\right]$$

$$= \frac{I_p}{5\tau}\left[V_d\, \tau\left\{1 - Exp\ (-5)\right\} + \frac{\tau R_s\, I_p^2}{2}\left\{1 - Exp\ (-10)\right\}\right]$$

$$= \frac{V_d\, I_p}{5}\left[1 - Exp\ (-5)\right] + \frac{R_s\, I_p}{10}\left[1 - Exp\ (-10)\right]$$

$$P_{av} \cong \frac{V_d\, I_p}{5} + \frac{R_s\, I_p^2}{10} \qquad [5.4]$$

In the present context the values of most interest are V_{ESD} (ESD voltage at which the device would damage) and the P_{av}/A (power density). From equation [5.3] V_{ESD} can be expressed by equation [5.5]

$$V_{ESD} = I_p\,(R_b + r_d + R_s + R_c) + V_d \qquad [5.5]$$

To determine the value of I_p, the equation [5.4] is solved in terms of P_{av} and the device parameters.

$$\frac{R_s}{10}\, I_p^2 + \frac{V_d}{5}\, I_p - P_{av} = 0$$

$$\therefore\quad I_p = \frac{-\frac{V_d}{5} \pm \sqrt{\left(\frac{V_d}{5}\right)^2 + 4\frac{R_s}{10} P_{av}}}{2\left(\frac{R_s}{10}\right)}$$

$$I_p = \frac{-V_d \pm \sqrt{V_d^2 + 10\, R_s\, P_{av}}}{R_s} \qquad [5.6]$$

Substituting [5.6] in [5.5]

$$V_{ESD} = V_d + (R_b + r_d + R_s + R_c)\left[\frac{-V_d \pm \sqrt{V_d^2 + 10\ R_s\ P_{av}}}{R_s}\right] \qquad [5.7]$$

A convenient method of determining the power density would be to plot equation [5.1] for different materials. The plot would approximate to a straight line and knowing the time constant, the P_{av}/A values can be read off the plot corresponding to 5 τ value. The plot[35] for reverse-biased (melting temperature, $T_m = 1412°C$) silicon junction semiconductors is shown in Fig. 5.25.

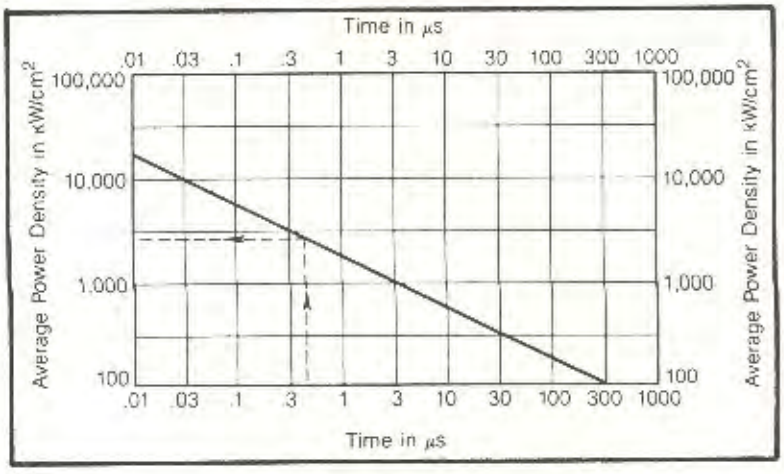


Fig. 5.25 – Average power density across a reverse biased emitter base junction (NPN transistor) causing failure of $\geq$ 5% of devices

The emitter base junction is most vulnerable to ESD damages because they are the smallest junctions in the circuit, and the bases and emitters are connected directly to external package leads and also the side walls of the emitter-base junction provide the lowest resistance current path. A reverse polarity (emitter positive) pulse of amplitude V_{ESD} can easily damage the device. Some of the factors affecting the junction damage are:

- Surrounding parasitics including parallel path devices.
- Bias condition of the previous junction.
- Junction doping concentration and doping profile[36]
- Pulse polarity.

6. AN EFFECTIVE ESD CONTROL PROGRAMME

The purpose of an effective ESD control programme is to eliminate any failures which can possibly be eliminated. There is no universal and magic formula which can provide the essential information and still be effective and economical. Depending upon the actual need and the ESDS items being processed the programme structure can widely vary. Normally an effective ESD control programme is very detailed and specific by nature. But the basic underlying concepts, as described in International Rectifiers handbook[15] for MOSFET may be summarised as below:

1. Always store and transport MOSFETs in *closed* conductive containers.
2. Remove MOSFETs from containers only after grounding at a Static Control Work Station.
3. Personnel who handle power MOSFETs should wear a static dissipative outer garment and should be grounded at all times.
4. Floors should have a grounded static dissipative covering or treatment.
5. Tables should have a grounded static dissipative covering.
6. Avoid insulating materials of any kind.
7. Use anti-static materials in one-time applications only.
8. Always use a grounded soldering iron to install MOSFETs.
9. Test MOSFETs only at a static controlled work station.
10. Use all of these protective measures simultaneously and in conjunction with trained personnel.

Irrespective of the manufacturing conditions and the general level of operator understanding and knowledge of ESD problems, the following five factors should be considered in designing an effective floor management programme:

1. The sensitivity of the components in use.
2. The physical areas to be protected.
3. The mobility of personnel and equipment.
4. The potential for management control.
5. The cost/benefit analysis.

Although an ESD control programme may be different for different industries, all the manufacturers agree that the approach to static control must be thorough and systematic, it must be thorough and systematic, it must include the entire manufacturing cycle, or else it will not work. It must also take into account ESD problems in handling, storing, shipping and retailing. If any phase is omitted, one might just as well throw away all the special materials and devices. Static-charge induced failures are well documented. In this respect two basic solutions have evolved:

1. If it moves, shield it.
2. If is does not move, ground it.

The two basic elements of static control plan are protection and grounding. Any static control programme must begin with protection of devices. Incoming static sensitive devices must be protected by conductive packaging materials. Grounding is essential to prevent static charge from developing. Grounding should never be direct (hard ground). It is recommended that the minimum resistance to ground must be 1 M-ohm. In other words the grounding should always be soft and never hard.

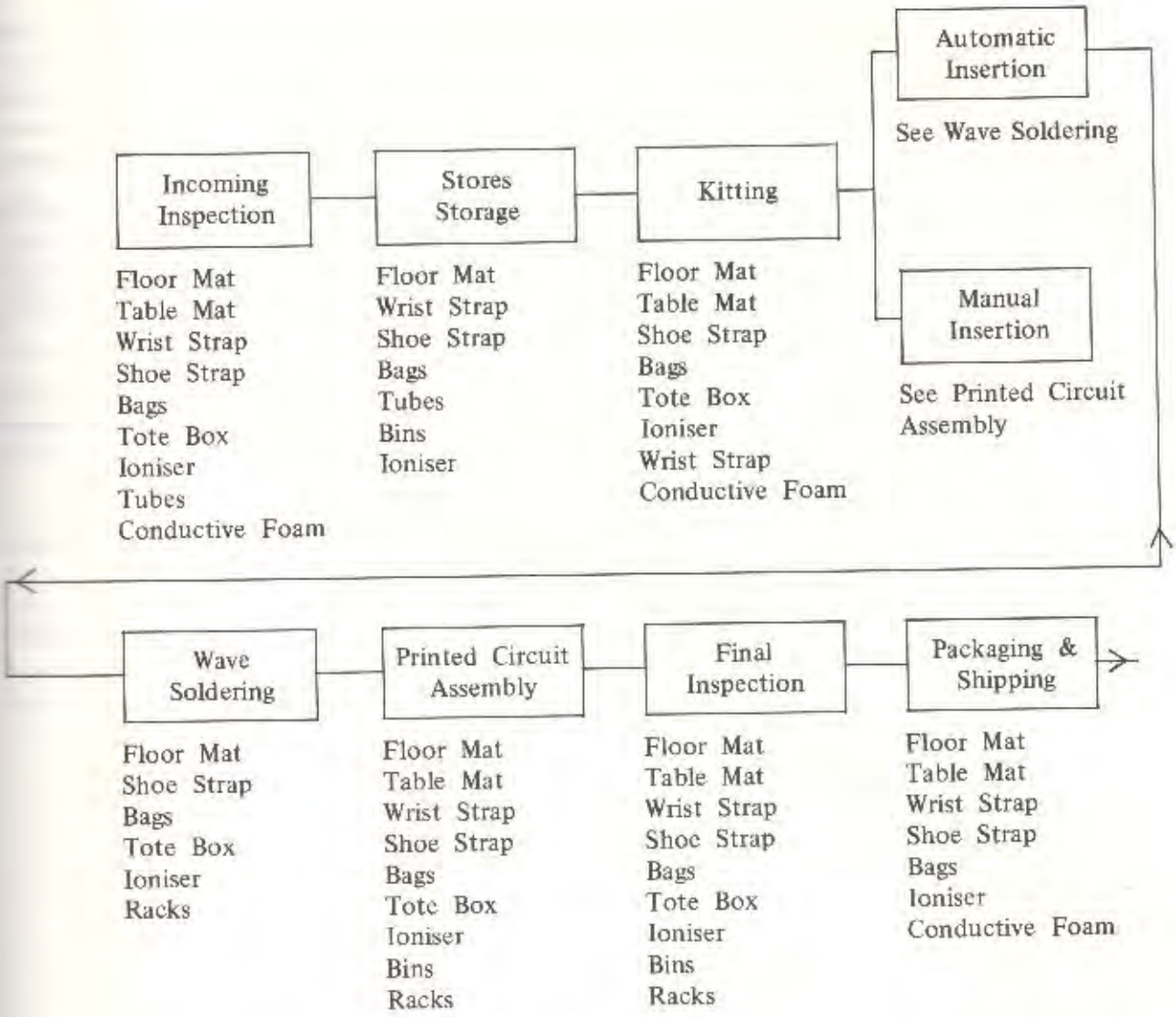


Figure 6.1 – Typical static problem areas and their solutions.

The movement of ESDS items should be studied to identify the problem areas. Having located the source and the extent of the problem the solutions can be provided. A block diagram indicating the static problem areas and their solutions is given in Fig. 61.

Matisoff[37] has summarised the requirements of an effective ESD programme, the details are are given below. The detailed implementation of an ESD programme as per to the recommendations made in DOD-HDBK 263 and DOD-HDBK 1686 is separately done. The materials to be used in the programme and how to select a suitable material is also done in the subsequent sections. The summary is as below:

1. Your ESD control plan must begin at your vendor's plant. All sensitive devices should be shipped to you in conductive packaging material.

2. Receiving and inspection operations should be performed only in a grounded, ionised environment. No personnel should be allowed to unpack or handle sensitive devices in any other than this protective environment.

3. As your static-sensitive devices are transported throughout your operation, they should be packaged in a conductive container. Likewise, if you are utilising hand carts, the wheels should be made of conductive material. If not, a drag chain can be installed to keep each metal cart grounded as it is moved throughout your plant. Automatic transfer devices, such as conveyer belt should be augmented by ionising equipment located at all transfer points.

4. Assembly stations should be totally grounded. The work station itself should be a conductive material. The operator should be required to wear a wrist strap and stand on a conductive floor mat. An ioniser should be used to neutralise all devices and materials coming into the work area. Special assembly equipment, such as rail assembly stations, must be covered with ionisers, and both the station and the operator must be grounded.

5. Process machinery must be grounded. Sensitive devices and PC Board assemblies entering and leaving processed equipment should be exposed to an ionisation unit before and after processing. If a conveyer belt is used to transfer the device through the processed equipment, it should be protected with an ioniser to ensure that the conveyer belt stays static-free.

6. Finally, as the completed product is ready for shipment to either the end user and/or sister plant, it should be neutralised and then packaged in a conductive container. This packaging operation should be carried out in a complete work station including all grounding devices and ionising equipment.

7. FACTORS AFFECTING ESD

Electrostatic discharge embodies two processes; one in which charges are stored and the other in which these charges are drained off. The electrostatic energy is stored either in the device capacitance or the capacitance of a human body and is discharged to ground via the resistance in the discharge path. This resistance may include either one or the combination of body resistance, device resistance and contact resistance. The capacitance is largely determined by the relative permittivity of the material and the physical dimensions of the capacitance. The resistance is determined by the conductivity, surface and volume resistivities. The product of capacitance and resistance determines the rate at which the stored charges decay. For device and personnel safety the voltage should reduce to 100 V from 5000 V within 2 seconds. This is the requirement of Federal Test Method Standard 101, Test Method 4046. Thus any situation internal, to device or equipment, or external which can influence the values of capacitance and conductance will affects ESD.

The main influencing factors could be either inherent to design or process or external. The inherent factors are mostly unavoidable due to the very nature of the requirements. For example miniaturisation of active devices means reduction in power density which can be safely dissipated away and thus making it more vulnerable. Thus size reduction is one of the inherent factors. For MOS devices reduced oxide layer thickness is required to enhance the speed of working but this again makes it more vulnerable to ESD. The solution to these problems can only be obtained by improving the design and incorporating protection circuits. Ideally one needs better materials and processes.

Among the external factors affecting ESD are:

(1) Absolute and relative humidity.

(2) Temperature

(3) Relative humidity and temperature combination.

(4) Velocity

(5) Contact pressure and area.

(6) Orientation of parts.

(7) Polarity of charged sources.

(8) Human Ignorance

By far the most critical single factor affecting ESD is humidity which influences both permittivity and conductivity. One of the most common methods for draining charges is to increase the humidity of the air. This method is widely used in a number of industries, when the humidity is increased the electrostatic charges leak away through the moisture film absorbed on the charged surfaces [38]. The conductivity of moist air is almost the same as that of the dry air.

For proper understanding of the effects of humidity on ESD it is essential that we clearly establish the relationship between the two.

ABSOLUTE VS RELATIVE HUMIDITY.

The absolute humidity is the quantity of water vapour in a unit volume (g/cm^3). The relative humidity compares the actual humidity to the maximum humidity that is possible at the actual temperature, expressed as a percentage. Thus the quantity of vapour in a closed room at a given temperature determines the relative humidity. If the temperature increases, the relative humidity will decrease and vice-versa, while absolute humidity does not change. The dielectric strength of the air increases with increasing absolute humidity. From the point of view of electrostatics relative humidity is more important, it is generally measured and reported as percentages. If the relative humidity in a room is high, a thin layer of moisture is formed on the surface of a solid materials. This assists in draining off the charges by reducing the surface resistivity of the material. The deposi-

tion of the moisture film depends upon whether the material is hydrophobic or hydrophilic. For hydrophilic materials on which a continuous layer can be formed there would be no static problem.

EFFECT OF TEMPERATURE VARIATION ON RELATIVE HUMIDITY (RH)

While interpreting the published and measured RH values much care is needed, as it is normally done in open air. The temperature difference between either a heated or an air-conditioned building could be enough to significantly alter the RH values. Equation [7.1] can be used to calculate RH values at temperature T_2, if RH values at a lower temperature T_1 are known.

$$(RH)_2 = (RH)_1 \left(\frac{T_2}{T_1}\right)\left[\text{Exp} \quad c\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right] \qquad [7.1]$$

where

$(RH)_2$ = RH at temperature T_2

$(RH)_1$ = RH at temperature T_1, ambient outside temperature

C = 5370 for $-\ 20°C \leqslant T \leqslant +\ 70°C$

T_1 and T_2 = Temperatures in Kelvin

A plot of equation [7.1] is shown in Fig. 7.1. It can be seen from the graph that RH values decreases as the temperature inside the building increases. For example, on a day when the outside temperature is 10°C the RH value of 50% reduces to only about 22% when the temperature in a heated building reaches to 22°C. This means a considerable reduction in the conductivity with increased probability of ESD risk.

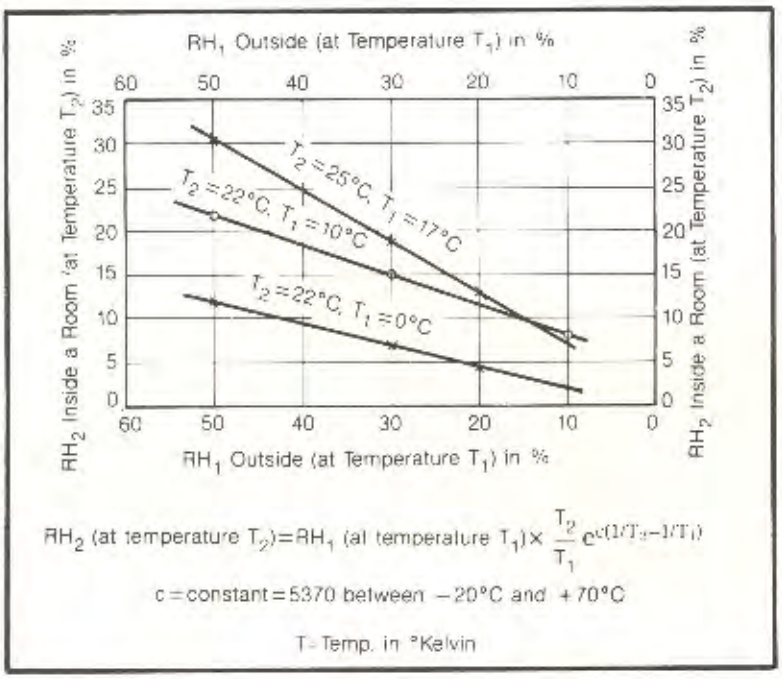
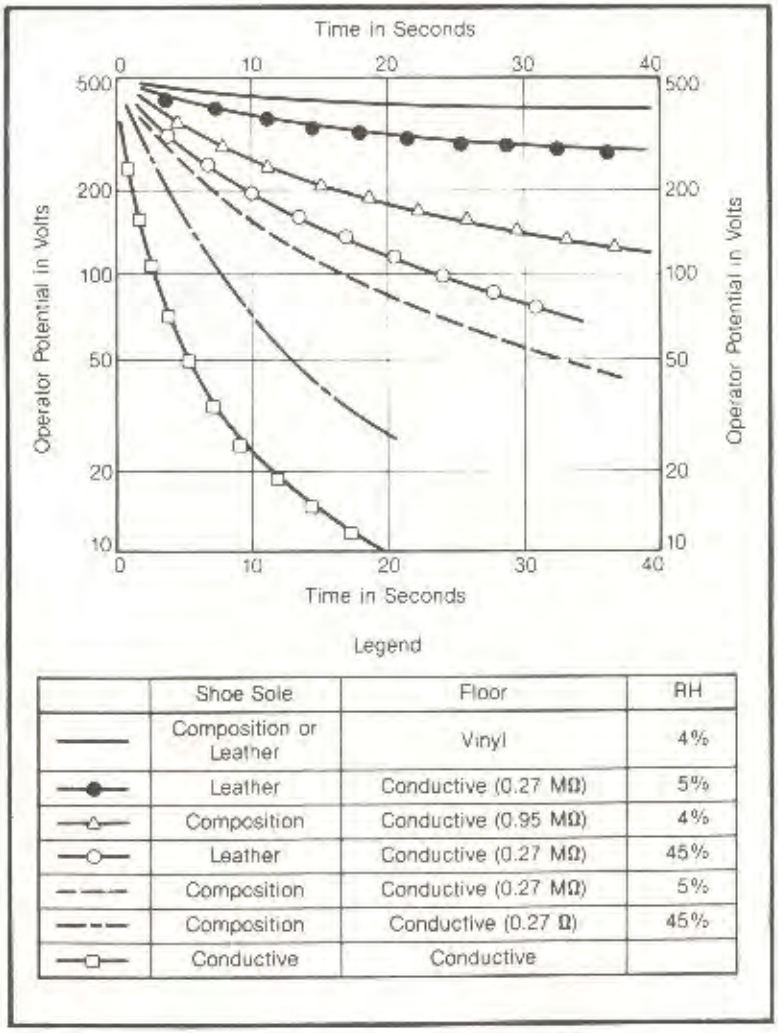


Figure 7.1 – Actual vs. apparent relative humidity.

EFFECT OF RELATIVE HUMIDITY ON STORAGE AND DECAY OF ELECTROSTATIC VOLTAGES

Manufacturers find that during winter and spring season the failure rate of integrated circuit is increased. Field and service engineers reports confirm the findings. Speakman[7], Kirk[3] and Yenni [40] and many others have reported that a significant increase in operator potential is observed when the RH values reduce. The graphs and charts in Figs. 7.2, 7.3 and 7.4 clearly display the effect of RH and material on ESD. The variation in ESD voltages, measured by Mc Farland [41] in a U.S.A.

works, given in Table 7.1, indicate that the voltages can increase by a factor of 15 for changes in RH values from 55% to 10%. This gives a rather hopeless picture of ESDS item when the sensitivity values of some known devices are looked at.



	Shoe Sole	Floor	RH
———	Composition or Leather	Vinyl	4%
—●—	Leather	Conductive (0.27 MΩ)	5%
—△—	Composition	Conductive (0.95 MΩ)	4%
—○—	Leather	Conductive (0.27 MΩ)	45%
– – –	Composition	Conductive (0.27 MΩ)	5%
– – –	Composition	Conductive (0.27 Ω)	45%
—□—	Conductive	Conductive	

Figure 7.2 – Electrostatically generated voltages decay at a rate that is dependent on relative humidity, type of floor covering and type of clothing worn by personnel. Decay times can take several minutes to reach safe levels

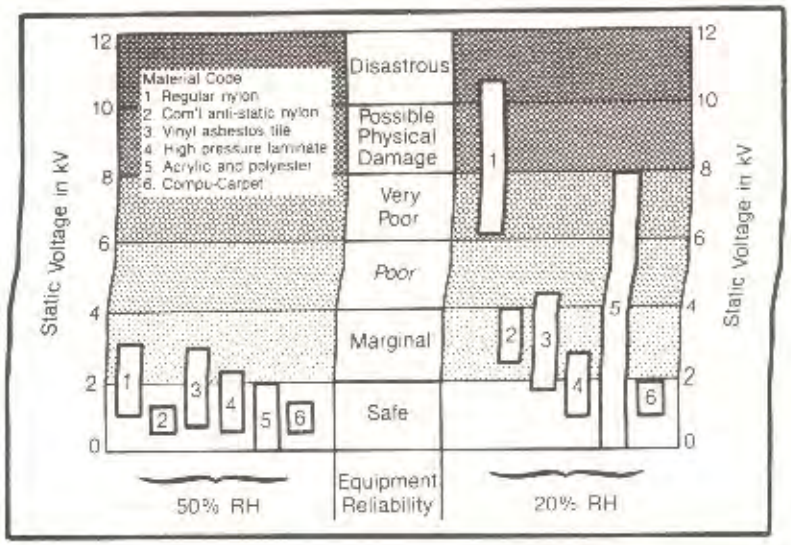


Figure 7.3 – Typical static voltages generated by walking on common floor covering materials

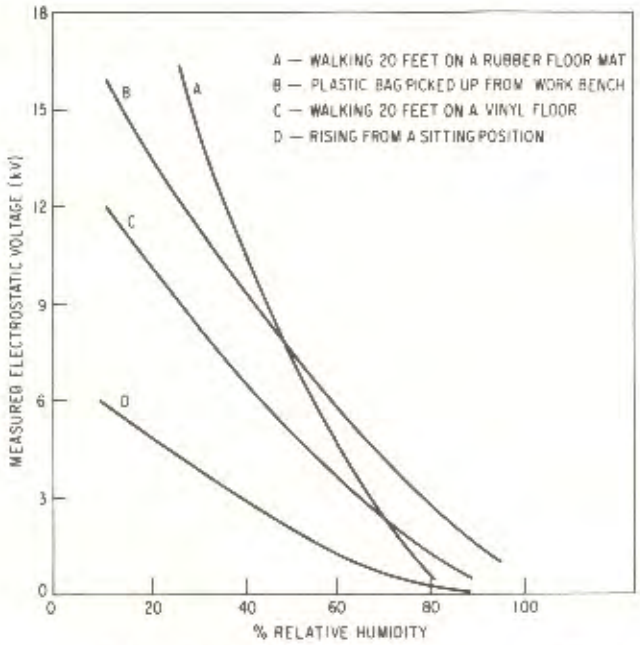


Figure 7.4 – Typical electrostatic voltages at different relative humidities.

TABLE 7.1 – ESD VOLTAGE MEASUREMENTS

MEANS OF STATIC GENERATION	ELECTROSTATIC VOLTAGES		
	10% R.H.	40% R.H.	55% R.H.
PERSON WALKING ACROSS CARPET	35,000*	15,000	7,500
PERSON WALKING ACROSS VINYL FLOOR	12,000*	5,000	3,000
WORKER AT A BENCH	6,000*	800	400
CERAMIC DIPS IN PLASTIC TUBE	2,000	700	400
CERAMIC DIPS IN VINYL SET-UP TRAYS	11,500	4,000	2,000
CERAMIC DIPS IN STYROFOAM	14,500	5,000	3,500
CIRCUIT PACKS AS BUBBLE PLASTIC COVER REMOVED	26,000	20,000	7,000
CIRCUIT PACKS AS PACKED IN FOAM LINED SHIPPING BOX	21,000	11,000	5,500

* VALUES CONFIRMED BY DOD-HDBK-263 DATED 5-2-80

To study the decay characteristics of static voltage as a function of RH Calderbank [42] did a series of tests to determine the degree of transfer of electrostatic charge from humans to a simulated printed wiring boards (PWB) assembly. The effects of clothing and floor coverings were also investigated. The results indicate that the transferred charge is significantly less than expected. The effects of humidity on charge accumulation and charge transfer on clothing were as expected i.e. higher humidities less charges.

The experimental set up used by calderbank et. al. is shown in Fig. 7.5. The clothing variations on the tests subjects is given in Table 7.2. The following experiments were performed:

(1) Charge generated and transferred as a result of walking.

(2) Charge generated and transferred as a result of rising from sitting position.

(3) Voltage decay rates of a human who had been charged to a known voltage.

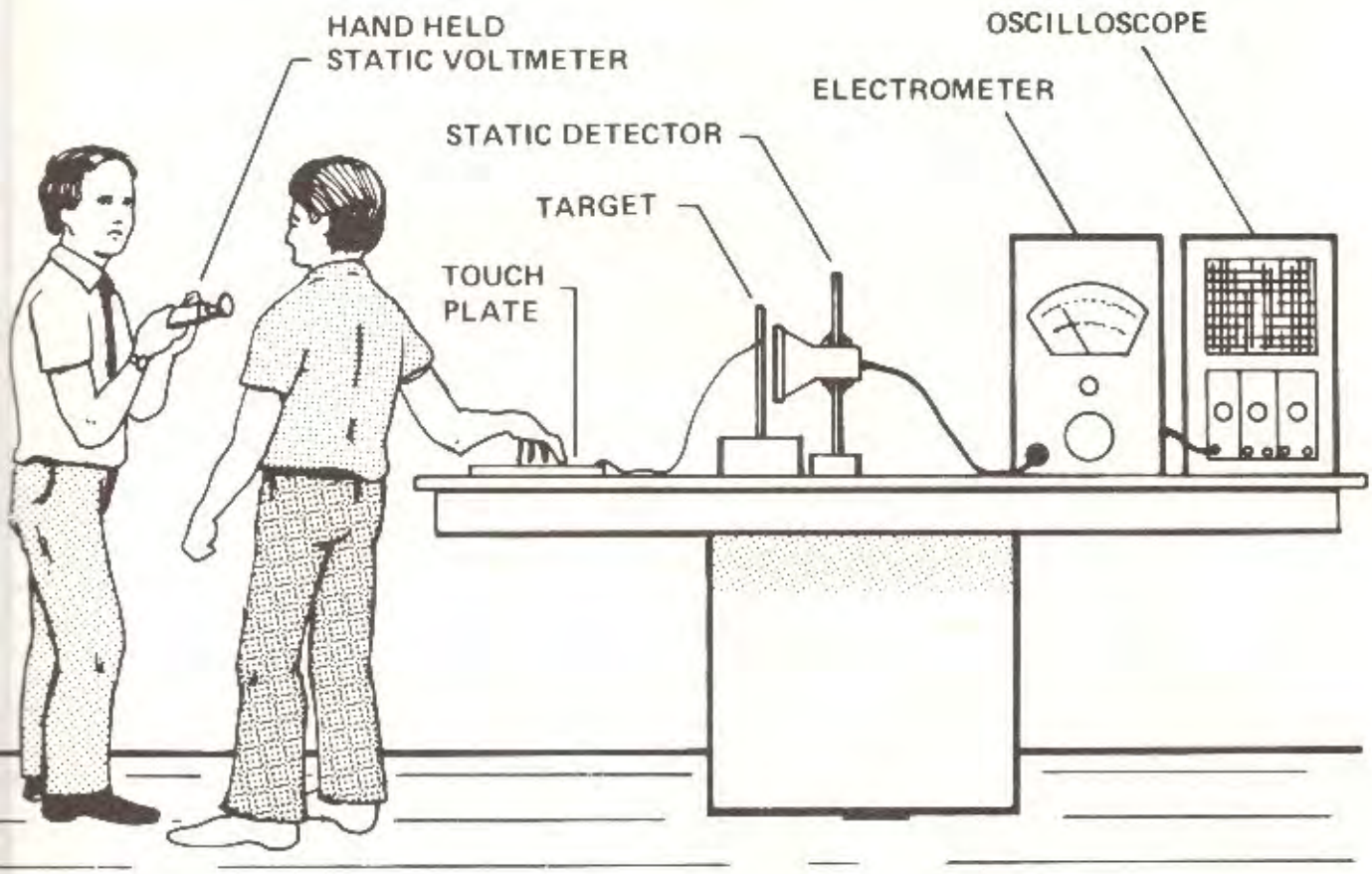


Figure 7.5 – Test Set-up

TABLE 7.2 – CLOTHING VARIATIONS ON TEST SUBJECTS

Test Subject	Clothing	Relative Humidity 35%	45%	55%	65%
1 Ralph	Shoes	Leather	Composition	Composition	Composition
	Shirt	Synthetic/Cotton	Synthetic/Cotton	Synthetic/Cotton	Synthetic/Cotton
	Pants	Synthetic	Synthetic	Synthetic	Synthetic
2 Don	Shoes	Leather	Leather	Leather	Leather
	Shirt	Synthetic/Cotton	Synthetic/Cotton	Synthetic/Cotton	Synthetic/Cotton
	Pants	Synthetic	Synthetic	Synthetic	Synthetic
3 Nancy	Shoes	Composition	Composition	Composition	Composition
	Shirt	Synthetic/Cotton	Synthetic/Cotton	Synthetic	Synthetic/Cotton
	Pants	Synthetic	Cotton	Synthetic	Synthetic
4 Frank	Shoes	Leather	Leather	Leather	Leather
	Shirt	Cotton	Cotton	Cotton	Cotton
	Pants	Synthetic	Synthetic	Synthetic	Synthetic
5 Connie	Shoes	Composition	Composition	Composition	Composition
	Shirt	Synthetic	Cotton	Cotton	Cotton
	Pants	Synthetic	Cotton	Synthetic	Synthetic/Cotton
6 Debbie	Shoes	Composition	Composition	Composition	Composition
	Shirt	Cotton	Cotton	Cotton	Synthetic/Cotton
	Pants	Synthetic	Synthetic	Synthetic	Synthetic

Experiment number one was conducted on two floor surfaces (bare concrete and rubber mat) at four relative humidities (35%, 45%, 55% and 65%). The details of experiment number one and the other two experiments are given in Table 7.3. The results of experiment number one and two are given in Table 7.4 and that of experiment number three in Fig. 7.6, 7.7 and 7.8. The conclusions drawn from the results of the experiments are:

(1) Electrostatic charges transferred from the human body to assemblies or devices through normal handling were found to be less than the charges measured on the clothing.

(2) The relative humidity does not appear to affect the charge transfer until it exceeds the comfort zone (35%, 45% and 55%).

(3) Clothing only slightly affects the magnitude of the transferred charge.

(4) In the entire range of the experiment (except for the Teflon data), only 3% of all transferred charges exceeded 100 Volts, and less than 1% exceeded 200 Volts.

TABLE 7.3 – TEST MATRIX

DESCRIPTION OF EXPERIMENT	Floor Surface			Relative Humidity					Experiment Designation
	A Bare Concrete	B Rubber Mat	C Teflon Plate	35%	45%	55%	65%	75%	
1. Walking approximately 20 feet before touching plate	•			•	•	•	•		1A
		•		•	•	•	•		1B
2. Rising from a sitting position before touching plate	•			•	•	•	•		2A
		•		•	•	•	•		2B
			•	•			•		2C
3. Voltage decay rates	•			•	•	•	•	•	3A
		•		•	•	•	•	•	3B
			•	•	•	•	•	•	3C

TABLE 7.4 – TEST RESULTS

	Condition	Measured	Relative Humidity			
			35%	45%	55%	65%
Floor Surface	Bare Floor (1A, 2A)	Shirt	400	370	110	0
		Pants	3.5k	1.5k	1.5k	500
		XFER	19	31	21	3
	Rubber Mat (1B, 2B)	Shirt	300	330	200	0
		Pants	2.7k	1.4k	1.5k	500
		XFER	21	27	29	3
	Teflon (2C)	Shirt	583	---	---	41
		Pants	2.9k	---	---	250
		XFER	908	---	---	7
Shoe Soles	Leather (1A,1B,2A,2B)	Shirt	200	600	90	0
		Pants	2.6k	2.3k	1k	500
		XFER	16	17	18	1
	Composition (1A,1B,2A,2B)	Shirt	450	200	190	0
		Pants	3.4k	1k	1.3k	500
		XFER	27	41	29	4
Action	Walking (1A, 1B)	Shirt	300	300	150	0
		Pants	3.0k	1.3k	1.5k	500
		XFER	18	18	15	3
	Rising (2A, 2B)	Shirt	360	400	160	0
		Pants	2.9k	1.6k	1.5k	500
		XFER	22	40	36	3

Average Measured Voltages

Relative Humidity			
35%	45%	55%	65%
4k	2k	1k	0
12k	7k	8k	4k
150	400	120	30
2k	2k	1k	0
13k	5k	8k	4k
100	100	120	30
1.3k	---	---	100
13k	---	---	1.5k
4k	---	---	50
1.1k	2k	500	0
8k	5k	4k	2k
120	60	60	10
4k	500	1k	0
13k	7k	8k	4k
150	400	120	30
2.5k	2k	1k	0
10k	5k	8k	4k
150	100	80	30
4k	2k	1k	0
13k	7k	8k	4k
150	400	120	30

Maximum Measured Voltages
(Minimum = 0 in all cases)

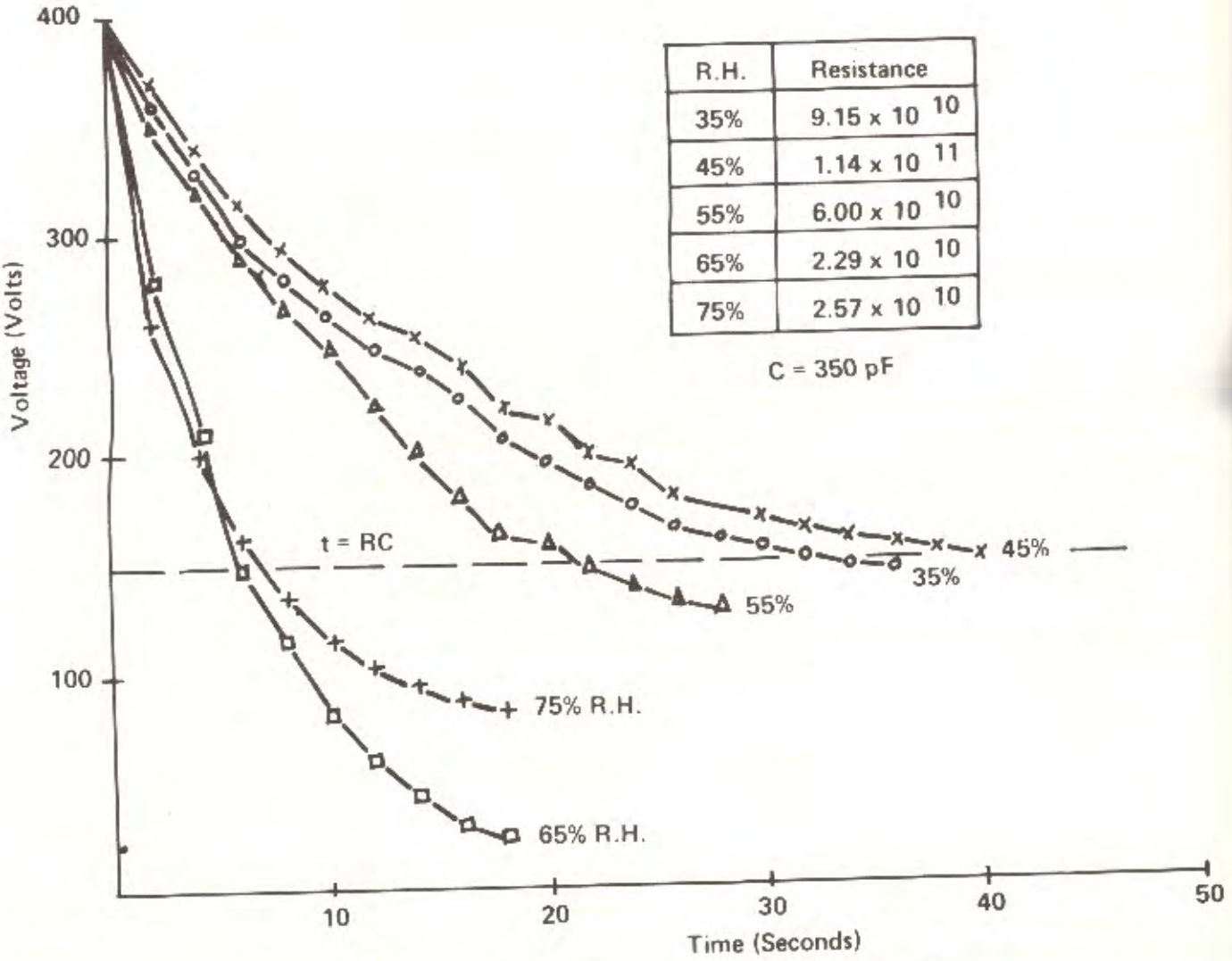


Figure 7.6 — Decay Voltage vs. Time; Composition Soles, Bare Floors.

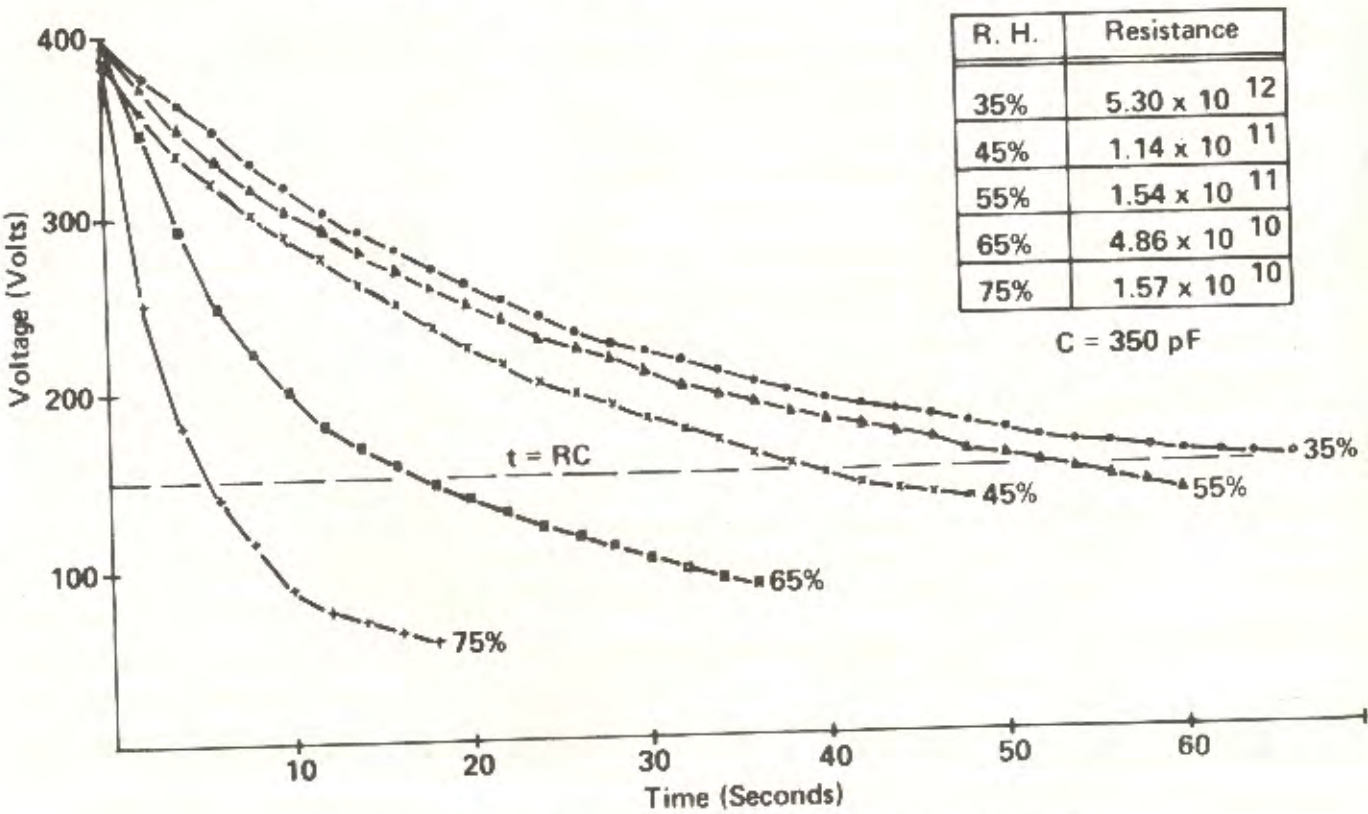


Figure 7.7 — Decay Voltage vs. Time; Composition Soles Rubber Mat.

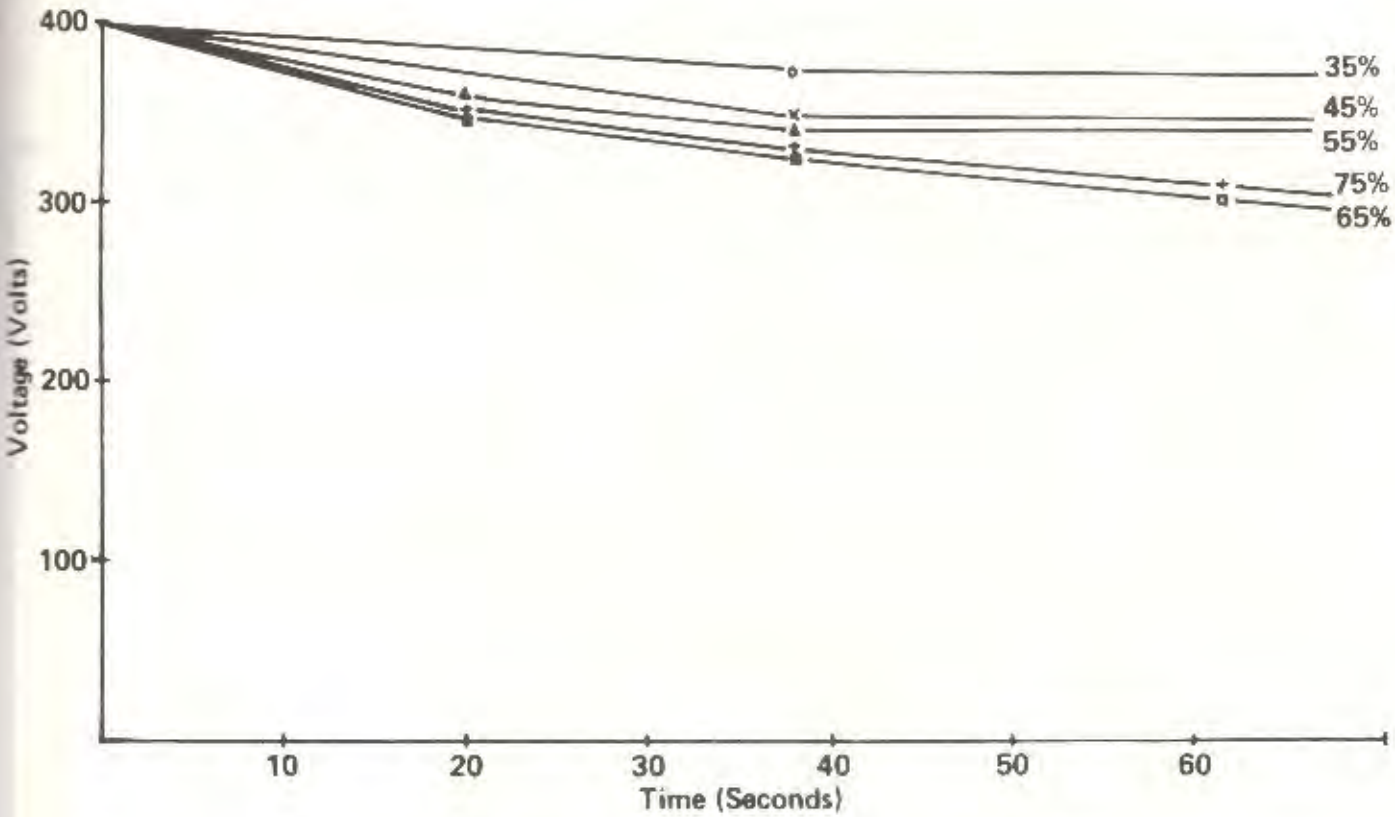


Figure 7.8 – Decay Voltage vs. Time; Composition Soles, Teflon Plate.

SEASONAL VARIATION IN RELATIVE HUMIDITY AND ITS EFFECT ON DEVICE FAILURE RATE

In the previous section we have seen that a reduction in RH values can mean a significant increase in ESD potentials acquired by charge storing items. Manufacturers have observed a significant variation in failure rates during the different seasons of the year. This is particularly true of manufacturing plants located in cold countries. To indicate the extent of problems due to seasonal variation in RH values Table 7.5 is given. The data clearly suggests that the relative humidity values in some states drops below 20%. This in itself may not appear very harmful but much care is needed before relaxing over it. Because the RH values inside the airconditioned or heated buildings will be much lower. McAleer[43] et. al studied the effect of various factors on ESD induced damage over a one year period. They reported that the uncontrolled relative humidity in West Texas ranges from 30% in the winter months to 60% in the summer. Ideally RH should be maintained at 50% plant wide and up to 65% in ESD sensitive areas. Obviously this calls for the use of humidifiers.

The variations in internal plant humidity measured by McAleer for 1979 and 1980 is given in Fig. 7.9 and the effect such humidity variations on the failure rates of CMOS devices is shown in Fig. 7.10. With the exception for Dec 1980, the graph shows the cyclic nature and relationship of MOS line failure and level of relative humidity.

While there is common understanding that higher relative humidity in the work area means reduced ESD induced failers Blinde[44] et. al. report that it is not sufficient to specify environmental ESD protection in terms of absolute humidity; nor is a relative humidity specification sufficient since temperature affects ESD parameters other than atmospheric moisture content. Accordingly, selection of the proper environmental conditions for appropriate ESD control requires selection of the appropriate discharge decay time constant ($G+=ae^{b(H)}$) value and a specification of the material. Only then can the optimum relative humidity or absolute humidity, and temperature be selected. In the equation for G, a and b are found to be temperature dependent constants different for absolute and relative humidity.

The second most important factor which affects ESD is the human ignorance and tendency of refusing to accept that it can be a real economic killer. It is therefore essential to organise talks, seminars, workshops, video shows etc to make every one aware of the problem, how it is caused and how it can be controlled. Any ESD protection programme must be total and must include every one involved. The committment from top management in removing such ignorance is necessary. It is therefore important that an awareness programme must be started with the most senior management responsible for allocating budget. Statistically only 10% of the ESD problems result in hard, or confirmed, failures, 90% of the ESD strikes remain subliminal and result in "walking wounded". The programme then should be suitably adjusted for engineers, supervisors and workers. Workers must be shown the effect of not following the ESD instructions.

The storage and decay of static charge depends on the speed at which two materials are separated. This depends on the characteristics of the materials being separated.

The effect of orientation and polarity of the discharging pulse has been discussed earlier. Contact pressure and contact area tend to affect the contact resistance. The contact resistance comes in the discharge path and determines the time constant or the pulse width of the discharge pulse.

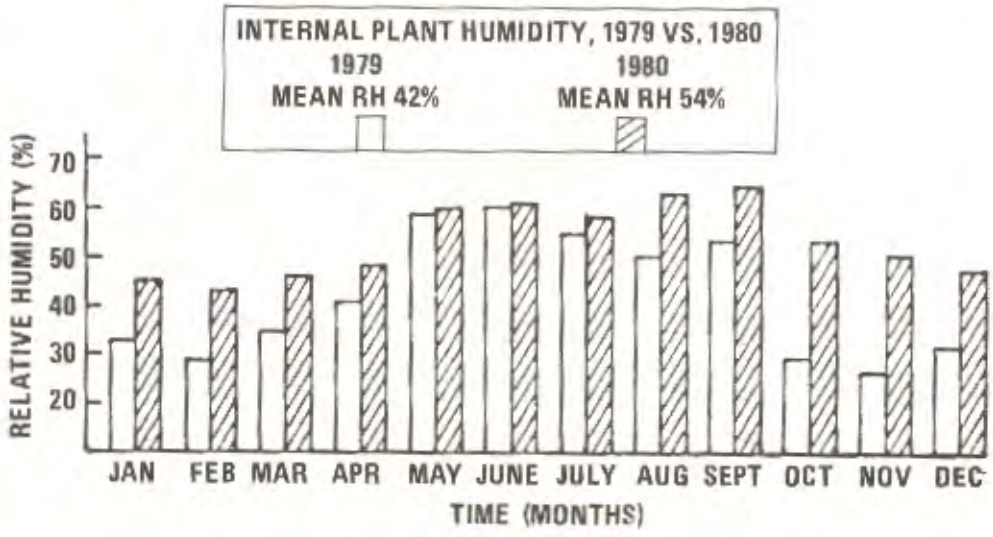


Figure 7.9 – Measured Relative Humidity

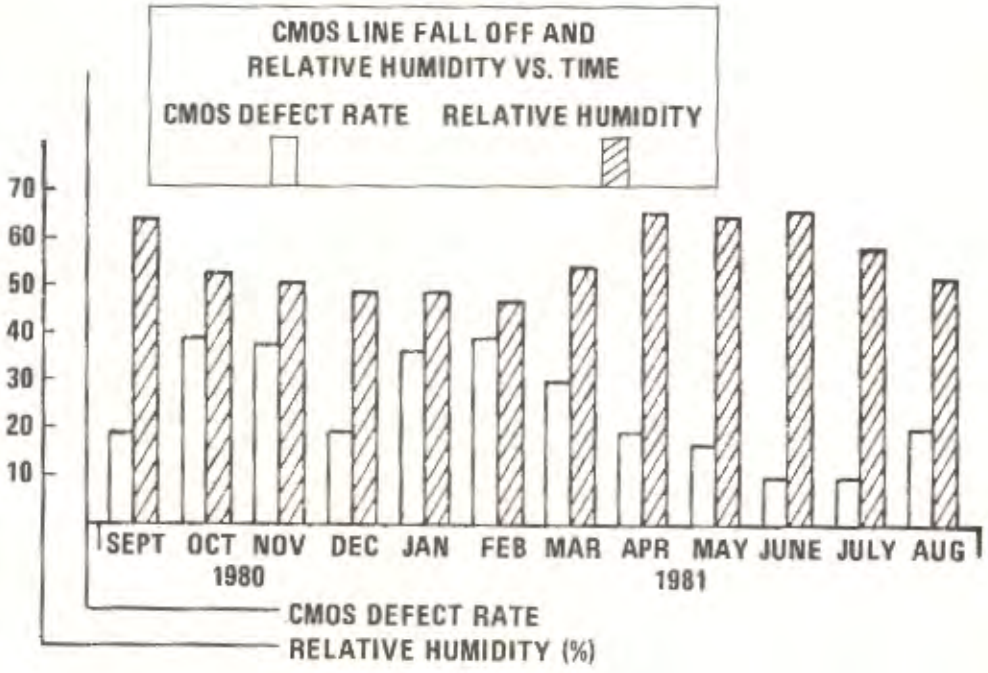


Figure 7.10 – Effect of Relative Humidity on Failure Rate of CMOS Devices.

TABLE 7.5 – RELATIVE HUMIDITY IN SELECTED U.S. CITIES

STATE	STATION	Length of record (yr.)	Jan		Mar		May		July		Sept		Nov		Annual	
			7:00 a.m.	1:00 p.m.	7:00 a.m.	1:00 p.m.	7:00 a.m.	1:00 p.m.	7:00 a.m.	1:00 p.m.	7:00 a.m.	1:00 p.m.	7:00 a.m.	1:00 p.m.	7:00 a.m.	1:00 p.m.
Ala	Mobile	17	81	62	83	56	86	54	89	61	88	61	85	56	85	57
Alaska	Juneau	36	79	75	79	69	74	62	81	70	87	77	85	81	81	73
Ariz	Phoenix	19	45	(32)	33	(23)	18	(13)	28	(20)	31	(23)	37	28	32	22
Ark	Little Rock	19	80	62	78	56	86	57	87	58	89	59	82	57	83	57
Calif	Los Angeles	20	56	60	62	65	66	66	69	68	66	67	57	63	62	65
	Sacramento	19	85	70	68	52	50	36	47	28	50	31	75	59	63	46
	San Francisco	20	79	67	70	63	64	60	66	60	65	59	73	64	69	62
Colo	Denver	19	45	48	42	40	39	37	(35)	35	38	(34)	45	50	40	40
Conn	Hartford	20	72	57	72	53	73	47	79	51	87	58	80	57	77	53
Del	Wilmington	32	75	60	74	53	76	53	80	54	85	56	80	56	78	55
D.C	Washington	19	68	54	68	49	72	51	76	53	80	56	74	53	73	52
Fla	Jacksonville	43	87	57	85	49	84	50	88	58	91	62	89	55	87	55
	Miami	15	84	60	82	56	82	61	85	64	89	68	85	61	84	62
Ga	Atlanta	19	78	60	78	51	83	55	90	63	90	61	82	54	83	57
Hawaii	Honolulu	10	80	83	73	58	67	55	66	51	66	52	74	59	71	56
Idaho	Boise	40	73	70	55	44	45	34	33	(21)	39	(30)	65	60	52	44
Ill	Chicago	21	76	68	79	62	76	54	81	57	84	57	80	64	79	60
	Peoria	20	77	68	81	64	81	57	85	58	88	58	83	66	82	61
Ind	Indianapolis	20	81	70	80	63	82	57	87	60	91	59	85	67	84	62
Iowa	Des Moines	18	76	68	78	63	78	55	81	57	84	59	79	64	80	61
Kans	Wichita	26	79	63	76	54	83	55	78	49	82	55	79	57	79	55
Ky	Louisville	19	77	65	76	59	83	56	86	59	89	60	79	61	81	59
La	New Orleans	31	85	67	85	61	89	60	91	66	89	66	86	61	88	63
Maine	Portland	39	77	62	75	58	75	58	80	60	86	61	84	63	80	60
Md	Baltimore	26	71	58	71	51	77	53	82	53	85	56	77	55	77	54
Mass	Boston	15	68	58	68	57	71	58	73	56	79	61	75	61	72	58
Mich	Detroit	45	78	69	77	60	71	51	74	51	82	55	79	64	77	58
	Sault Ste. Marie	38	82	76	83	68	80	56	89	62	92	67	87	76	85	67
Minn.	Duluth	18	74	68	77	63	76	54	83	58	86	63	80	69	80	63
	Minneapolis-St. Paul	20	72	66	76	63	76	52	81	54	86	60	80	66	79	60
Miss	Jackson	16	87	66	88	57	92	56	93	60	94	61	91	58	91	59
Mo	Kansas City	7	74	65	78	62	83	59	82	56	86	60	78	62	80	60
	St. Louis	19	83	66	82	59	83	56	86	57	91	59	85	63	84	60
Mont	Great Falls	18	63	62	53	48	46	40	38	(29)	45	36	55	54	50	45
Nebr	Omaha	15	76	65	76	57	79	55	83	56	87	61	80	62	80	59
Nev	Reno	16	68	50	47	(33)	33	(25)	28	(19)	34	(21)	56	41	44	31
N.H	Concord	14	74	60	78	56	79	48	86	52	91	57	85	61	82	55
N.J	Atlantic City	15	75	58	76	55	79	57	84	58	86	59	82	57	80	57
N. Mex	Albuquerque	19	50	39	(32)	(23)	24	(17)	35	(27)	40	31	42	35	37	28
N.Y	Albany	14	79	64	74	54	76	52	80	54	88	59	81	63	79	57
	Buffalo	19	80	74	80	67	76	56	79	55	83	60	82	70	80	63
	New York	58	68	60	67	55	71	53	75	55	79	57	73	59	72	56
N.C	Charlotte	19	78	56	80	51	84	54	88	59	90	58	84	53	83	54
	Raleigh	15	79	55	80	49	87	56	90	59	93	60	85	51	85	54
N. Dak	Bismarck	20	72	66	78	62	79	49	83	47	82	49	79	62	79	56
Ohio	Cincinnati	17	79	68	77	60	80	54	85	57	88	59	80	63	81	60
	Cleveland	19	77	70	78	65	77	58	82	58	84	61	79	66	79	63
	Columbus	20	76	68	73	58	79	55	84	56	88	59	81	64	80	59
Okla	Oklahoma City	14	79	61	75	52	83	58	81	50	84	56	78	54	80	54
Oreg	Portland	39	82	76	72	60	66	53	61	45	67	49	82	74	72	60
Pa	Philadelphia	20	73	59	71	53	75	53	79	55	83	57	77	56	76	55
	Pittsburgh	19	78	66	74	58	76	51	82	53	86	57	79	63	78	57
R.I	Providence	16	72	58	70	54	72	52	77	57	82	57	78	59	75	55
S.C	Columbia	13	82	55	83	48	87	51	89	56	93	58	88	49	87	52
S. Dak	Sioux Falls	16	74	67	80	63	80	53	81	52	85	57	82	64	80	59
Tenn	Memphis	40	78	63	76	56	82	55	85	57	86	56	79	55	81	57
	Nashville	14	80	65	78	54	87	56	91	59	92	51	81	59	85	58
Tex	Dallas-Fort Worth	16	80	61	80	57	88	61	81	50	87	59	81	56	82	57
	El Paso	19	44	34	(28)	(20)	22	15	39	29	44	34	38	(32)	35	27
	Houston	10	88	66	89	60	94	60	94	59	95	65	91	60	92	60
Utah	Salt Lake City	20	70	68	52	45	37	(31)	26	(20)	34	27	57	58	46	42
Vt	Burlington	14	70	64	73	59	75	51	80	54	87	64	79	69	78	60
Va	Norfolk	31	75	59	74	54	78	57	82	60	84	62	79	56	78	58
	Richmond	45	81	57	78	49	79	51	85	57	90	57	85	50	83	53
Wash	Seattle-Tacoma	20	78	74	74	62	67	54	65	48	74	59	80	74	73	62
	Spokane	20	82	77	67	54	52	40	39	25	50	34	81	74	62	51
W. Va	Charleston	32	77	63	74	53	82	50	90	61	91	56	80	56	82	56
Wis	Milwaukee	19	75	68	79	66	79	61	82	61	87	63	81	57	81	65
Wyo	Cheyenne	20	45	48	44	40	39	41	(34)	37	35	36	42	47	40	42
PR	San Juan	24	80	84	77	60	77	65	78	66	79	67	81	86	79	84

Please note These figures given in percentages represent the averages for the period of record through 1979. Eastern Standard Times are indicated.

8. ELECTROSTATIC HAZARDS

In this section our main objective is to identify the hazardous aspects of ESD. First we will look in to the conditions which, may lead to hazards or, are known to have resulted in dangerous accidents when a programme to control the ESD was not used. Then we will look in to the conditions which will lead to hazards if recommended precaution are not observed even if an ESD control programme is in operation. Before we can discuss this issue, we must clearly know what do we really mean by hazard. Some may argue that nuisance can be hazardous and some might like to overlook even a deadly risky situation by saying it is unlikely to occur. Hazards range in magnitude from major hazards, with potential loss of life and possible damage costing millions of dollars, to minor annoyances in the home, office or factory. The problem includes explosion during handling, like the one experienced by Honeywell[45] when a primer exploded due to an inadvertent firing, filtering, refining and transportation. Losses in the manufacturing and handling of photographic film and electronic integrated circuits and devices may lead to major hazard or just a nuisance.

Hazards can be classified in a number of ways. However, according to one classification, accepted by most and used in evaluating the liability cost and compensation in aerospace industry, the hazards can be ranked as below:

- Class I Hazards : Negligible effects
- Class II Hazards : Marginal effects
- Class III Hazards : Critical effects
- Class IV Hazards : Catastrophic effects

ESD related hazard could fall in to any one of the above four classes. Fig. 8.1 lists some of the hazards and annoyances due to electrostatics.[46]

Some of the possible hazards of inadequately or improperly implementing the precautions in dealing with ESD problems are:

(i) Electric Shock
(ii) Fire
(iii) Explosion

By far the most serious problem in Electronic manufacturing is encountered when the human body itself becomes a part of the circuit and the level of current through the body increases beyond a few milliampere. The most direct method of protecting ESDS items is to drain off the static charge to ground by suitable grounding of the people, the work bench and the area of use. The safety requirements of MIL-STD-454G[47], should be followed in the construction of ESD protected areas where grounding is used to dissipate electrical charges. The general requirements are:

- Grounding should never be hard.
- The minimum resistance to ground should never be less than 1Mohm.
- RC time constant of the discharge path should be such that a human body charged to 5000V discharges to 100 V in less than two seconds i.e. it must comply with FED-STD 101B, Method 4046.[48]
- The exposure to electrical current should not be more than 5 milliampere.
- The conductive mat on the work bench should not be replaced by an equivalent resistor.

When looking into the possibility of electrical shock it is better to consider current rather than the voltage because of a wide variation obtainable in impedance of human bodies. Molinski [49] has identified the effects of the following six factors on the flow of current through a human body:

1. Type of circuit with which contact is made.
2. Voltage of the circuit.
3. Resistance of the discharge path including the body resistance.
4. Value of the current
5. Pathway of the current through the body.
6. Duration of the contact.

Table 8.1 shows the effect of ac main and d-c current on the human body [47]. The resistance needed to achieve a safe ground, following the recommendation of MIL-STD-454 G, can be calculated using equation [8.1]

$$\text{Safe resistance to ground} = \frac{\text{Highest attainable voltage by a worker}}{5 \times 10^{-3}} \quad \ldots\ldots\ldots\ldots [8.1]$$

Care must be taken to prevent isolation at any point in the grounding system of a static-controlled work area. A careful adherence to following points is advised:

(1) PCB turned over with the components facing down and laid on a foam pad creates an isolation point. The foam, therefore, should be conductive.

(2) All grounding should be complete to the safety ground in the facility electrical system, not earth ground.

(3) Stool covers should be used to eliminate isolation between the operator and the stool. Another point of isolation is the rubber casters on the stools.

Table 8.1 Effects of Electrical Current on the Human Body.

CURRENT VALUES IN MILLIAMPS		EFFECTS ON A HUMAN
AC (60 HZ)	DC	
0-1	0-4	Perception
1-4	4-15	Surprise
4-21	15-80	Reflex Action
21-40	80-160	Muscular Inhibition
40-100	160-300	Respiratory Block
Over 100	Over 300	Usually Fatal

It is known that upto a few kilovolts static voltage can be accumulated on various cloth and it is also accepted that the limiting energy for ignition of ordinary fuel vapours is 0.2 m Joule. To examine the effects of overalls of cotton, Terylene/cotton blends and nylon on fuel ignition a variety of experiments have been reported by Jowett [50]. The conclusion arrived at is that these materials can ignite gas mixtures at moderately low relative humidities, whilst nylon can do it over considerable ranges of humidity and gas concentration. A resistivity of 10^{11} ohm/□ for such garments is suggested.

HAZARDS CAUSED BY IONISERS

The degree of hazards due to the use of ionisers to neutralise the static charges depends on the type of ionisers and the degree of care taken in following the instructions. Hazards caused by ionisers can be divided into three main groups:

(1) Hazards with normal operation of ionisers.

(2) Hazards due to misuse of ionisers.

(3) Hazards due to poor housekeeping.

The hazards belonging to the first category are inherent in the operation and construction of the ionisers. For example the possibility of electrical shock, always exists because such ionisers use high voltage power supply to provide necessary ions. In case of radioactive ionisers the possibility of radiation hazards always exists. An ioniser without the current limiting circuit may be suitable in some situations, but in an inflammable atmospheres this type of ioniser may present an ignition hazard. Similary, a well constructed ioniser can cause net charging instead of neutralising, as a result of incorrect installation. All these constitute to hazards due to misuse. An ungrounded passive (induction type) ioniser will result in a hazard of the third type listed above. Further details on hazard due to ionisers can be found elsewhere[51].

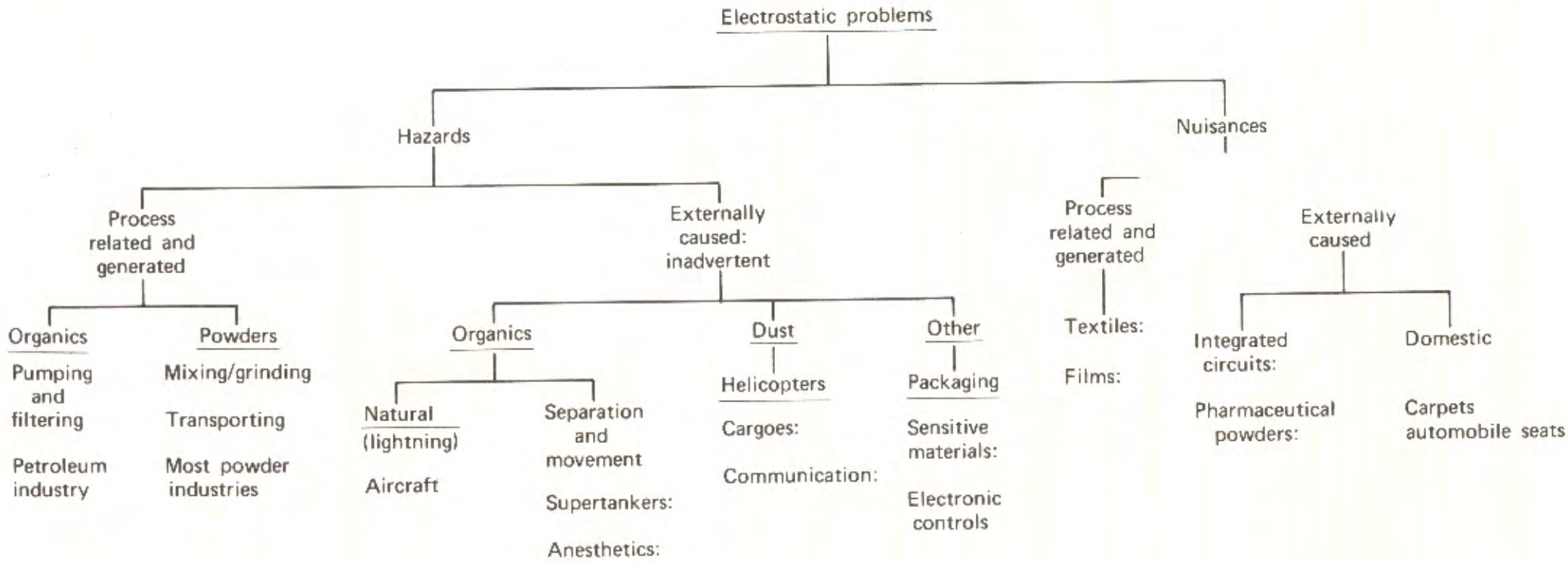


Fig. 8.1 – Some hazards and annoyance due to electrostatics

9. MODEL CALCULATIONS

The main objective here is to see how some of the analytical tools, developed to facilitate proper understanding of electrostatics related problems, are put to use. While performing these computations one would need to use from time to time the physics of semiconductor devices. In evaluating the level of protection required it often helps to remember, or at least keep them handy, some accepted facts and figures related to electrostatics. For example the requirement of decay time, minimum resistance to ground to be provided in the discharge path, requirement of MIL-STD-454 G, regarding the level of current through human body and minimum energy required to ignite fuel gases. These informations are readily available in the relevant standards.

In this section we would consider the following problems:

(1) Calculation of electrostatic energy stored in a human body.

(2) Calculation of decay time, knowing the values of volume resistivity and the thickness of the table top material.

(3) Calculation of range of electrostatic energy that can be stored in a human body.

(4) Application of Wunsch Bell model to calculate the power density dissipated at the Junction of a bipolar device which is known to have been damaged at a particular value of the voltage.

(5) Calculation of ESD sensitivity of a bipolar device subjected to charged bodies of different capacitance and resistance values.

Prob 1:

Calculate the electrostatic energy stored in a human body represented by the body capacitance of 100 PF and the body resistance of 1500 ohms and charged to 3000 volts. Calculate the time constant of the discharge path if device resistance is 10 ohms.

$$\text{Energy} = \frac{1}{2} CV^2$$

$$= \frac{1}{2} \times 100 \times 10^{-12} \times (3000)^2$$

$$= \frac{1}{2} \times 100 \times 10^{-12} \times 9 \times 10^6$$

$$= 4.5 \times 10^{-4}$$

$$= 0.45 \text{ m Joules}$$

This energy would discharge through a total resistance of $(R_b + R_s)$

$$\therefore \text{ Time constant } \tau = (R_b + R_s) C_b$$

$$= (1500 + 10) \times 100 \times 10^{-12}$$

$$= 1.510 \times 10^5 \times 10^{-12}$$

$$= 0.151 \text{ } \mu \text{ Second}$$

Time constant determines the rate at which the stored electrostatic energy would discharge to ground. 0.45 mJ would be enough to create enough overheating to fail the device as it is known that the energy needed, to vapourise silicon volume of 6 μm in diameter, is approximately 1 μJ.

Prob 2:

Calculate the resistance of the discharge path, for a person charged to 5000 V, consisting of a 100 square table top covered with a 0.05 cm thick material whose volume resistivity is 10^8 ohm cm. Assume that the finger and the ground lug contact is represented by 1 cm diameter. For the table top and floor mat capacitance of 200 pF, calculate the time taken to reach 100 V. Calculate the required surface resistivity so that the decay time is reduced to 2 seconds.

$$\text{Volume resistivity } \rho_v = R \frac{w}{l} t$$

where R resistance
w, l width and length of the material
t thickness of the material

for $w = l$

$$\rho_v = R\,t$$

and

$$\rho_s = R \qquad \text{ohm}/\square$$

$$\therefore \rho_v = \rho_s t$$

Neglecting the resistance of the human contact

$$R = \rho_s \times 100$$

$$= \frac{\rho_v}{t} \times 100$$

$$= \frac{10^8}{.05} \times 100 = \frac{10^{10}}{5} \times 10^2$$

$$= 20 \times 10^{10} \text{ ohms}$$

The discharge equation is:

$$V_t = V_o\, e^{-t/cR}$$

$$100 = 5000\, e^{-t/200 \times 10^{-12} \times 20 \times 10^{10}}$$

$$1 = 50\, e^{-t/40}$$

$$\therefore t = -40\, \ln (1/50) = 156.48 \text{ Second}$$

As a guide if the voltage level does not reach to 100 V within two seconds then the resistance of the table top and the floor mat must be reduced to provide good protection against ESD.

Let us now calculate the R value so that the decay time is 2 second.

$$\therefore -\frac{2}{200 \times 10^{-12} R} = \ln (1/50)$$

$$\therefore R = \frac{-2/200 \times 10^{-12}}{\ln (1/50)} = 2.556 \times 10^9 \text{ ohm}$$

$$\therefore \text{Surface resistivity for the mat, } \rho_s = \frac{2.556 \times 10^9}{100}$$

$$= 2.556 \times 10^7 \text{ ohm}/\square$$

This means a static dissipative material (10^5 ohm/□< ρ_s< 10^9 ohm/□) is required in this case.

Prob 3:

It is known that the capacitance of human body, depending upon age, sex, race, and size, can vary between 50 pF and 300 pF, calculate the range of electrostatic energy stored in human body if they are all charged to 5000 volts.

Energy stored $= \frac{1}{2} CV^2$

$\therefore$ Minimum energy stored $= \frac{1}{2} 50 \times 10^{-12} \times (5000)^2$

$= 6.25 \times 10^{-4}$ J

$= 0.625$ mJ

Maximum energy stored $= \frac{1}{2} 300 \times 10^{-12} (5000)^2$

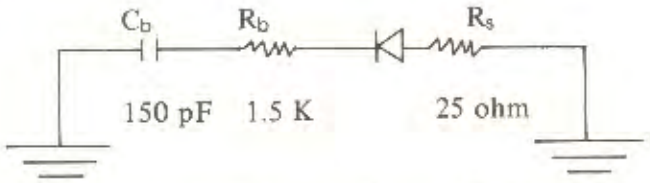
$= 3.75$ mJ

$\therefore$ Ratio of maximum to minimum energy stored $= \underline{6}$

The ratio of energy stored is the same as the ratio of human body capacitance.

Prob 4:

A bipolar silicon integrated circuit was damaged by human body (C_b = 150 pF and R_b = 1.5 K ohm) charged to 1000 V. If the bulk resistance of the semiconductor and the area of cross section of the junction were 25 ohm and 1.5×10^{-6} cm^2, calculate the power density at the junction. Neglect the contact resistance of the lead to ground and take the reverse breakdown voltage of the emitter base to be 10 V



Time constant τ = $(R_b + R_s) C_b$

$= (1500 + 25) \times 150 \times 10^{-12} = 228.75$ ns

$\therefore$ $5\tau = 750 \times 10^{-12} (1525) = 1.14375 \mu s$

From equation [5.3]

$$I_p = \frac{V_{ESD} - V_d}{R_b + R_s} = \frac{1000 - 10}{1525} = \frac{990}{1525} = 0.649 \text{ Amp}$$

From equation [5.4]

$$\text{Average Power, } P_{av} = \frac{V_d I_p}{5} + \frac{R_s I_p^2}{10}$$

$$\therefore \quad = \frac{10 \times 0.649}{5} + \frac{25 \times (0.649)^2}{10}$$

$$= 1.29836 + 1.05358 = 2.352 \text{ W}$$

Power density, $P_{av}/A = 1567.965 \text{ kW/cm}^2$

The value of P_{av}/A can also be obtained from the graph in Fig. 9.1 corresponding to time 1.144 μs.

From the Graph $P_{av}/A = 1600 \text{ kW/cm}^2$

It should be remembered that by definition V_{ESD} is the voltage at which the device will be damaged.

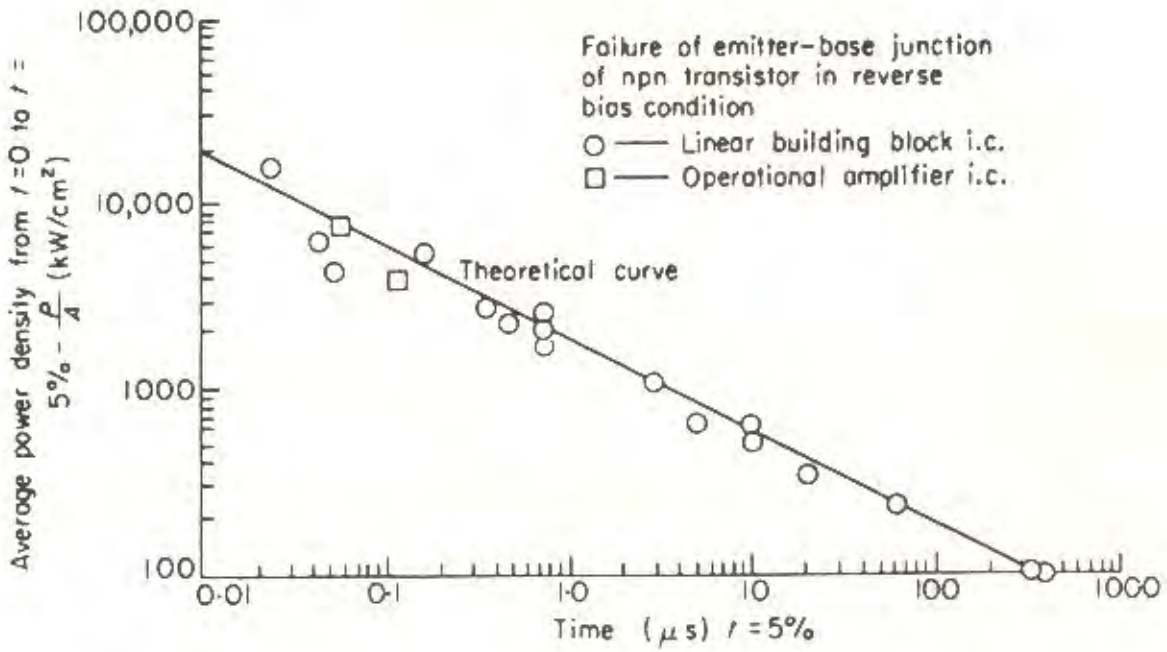


Figure 9.1 – Experimental data points superimposed on Wunsch-Bell curve.

Prob 5:

The capacitance and resistance values of ten workers in a plant manufacturing bipolar circuits of the following specification are given in Table 9.1. Which of the ten workers would damage the maximum number of devices.

Bulk resistance of emitter base region R_s = 25 ohms

Areas of Cross Section A = 1.5×10^{-6} cm^2

Reverse breakdown voltage V_d = 10 volts

Table 9.1

Worker Number	Body of Capacitance C_b (pF)	Body Resistance R_b (ohms)
1	50	500
2	300	500
3	50	30K
4	300	30K
5	140	2.1K
6	145	2.0K
7	140	2.1K
8	170	2.3K
9	180	1.9K
10	80	2.4K

In this case we need to calculate the minimum value of V_{ESD} which would damage the bipolar device.

We first need to calculate the time constant τ and then the value 5τ to calculate the average power using equations [5.1] and [5.4].

The time constants of the discharge path for ten workers will be given by $(R_b + R_s) C_b$. The τ and 5τ values are given in Table 9.2.

R_s = 25 ohms

Table 9.2

Worker	C_b PF	R_b ohms	τ $\times 10^{-9}$ s	5τ $\times 10^{-6}$ s
1	50	500	26.2	0.13125
2	300	500	157.5	0.7875
3	50	30k	1501.25	7.5062
4	300	30k	9007.5	45.05
5	140	2.1k	297.5	1.4875
6	145	2.0k	293.625	1.468
7	140	2.1k	297.5	1.4875
8	170	2.3k	395.25	1.976
9	180	1.9k	346.5	1.732
10	80	2.4k	194.0	0.97

Now two approaches can be used:

(1) Graphical: using the graph in Fig. 9.1 to find P_{av}/A.

(2) Analytical: using equation [5.1] for silicon.

Analytical Method:

For silicon the following values are used:

Thermal conductivity	k	=	1.412	watt $(cm\ k)^{-1}$
density	p	=	2.328	gm $(cm)^{-3}$
specific heat	C_p	=	0.7	J $(gm\ K)^{-1}$
Melting temperature	T_m	=	1412°C	
		=	1685 K	
Initial Temperature	T_i	=	25°C = 298 K	

$\therefore$ Equation [5.1] is reduced to:

$$P_{av}/A = \sqrt{\pi k\ C_p}\ (T_m - T_i)\ t^{-0.5}$$

$$= (3729.14)\ t^{-0.5}$$

$\therefore$ P_{av}/A and P_{av} for 10 workers are given in Table 9.3:

Worker	P_{av}/A kw/cm^2	P_{av} w
1	10293.4	15.44
2	4202.27	6.3
3	1361.13	2.042
4	555.6	0.833
5	3057.6	4.586
6	3077.84	4.617
7	3057.6	4.586
8	2652.87	3.979
9	2833.58	2.106
10	3786.37	5.679

Now we use equation [5.6] to determine the value of peak current I_p. The equation [5.6] is:

$$I_p = \frac{-V_d \pm \sqrt{V_d^2 + 10\ R_s\ P_{av}}}{R_s}$$

V_d = 10 V

R_s = 25 ohm

$\therefore$ $$I_p = \frac{-10 \pm \sqrt{100 + 250\ P_{av}}}{25}$$

The realistic and the only possible value will be:

$$I_p = \frac{-10 + \sqrt{100 + 250\ P_{av}}}{25}$$

For these 10 workers the I_p and V_{ESD} values given by $V_d + (R_b + R_s)\ I_p$ are given in Table 9.4:

Table 9.4

Worker	I_p Amps	V_{ESD} V
1	2.117	1121.42
2	1.845	978.62
3	0.878	26371.95
4	0.302	9077.55
5	1.515	3229.37
6	1.522	3092.0
7	1.515	3229.37
8	1.384	3227.8
9	0.898	1738.65
10	1.730	4207.67

Table 9.5 gives the results of the calculated values:

Table 9.5

Worker	C_b pF	R_b ohms	τ ns	5 τ us	P_{av}/A kw/cm^2	P_{av} watt	I_p Ap	V_{ESD} Volt
1	50	500	26.25	0.13125	10293.4	15.44	2.117	1121.42
2	300	500	157.5	0.7875	4202.27	6.3	1.845	978.62
3	50	30K	1501.25	7.5062	1361.128	2.042	0.878	26371.9
4	300	30K	9007.5	45.05	555.599	0.833	0.302	9077.55
5	140	2.1K	297.5	1.4875	3057.6	4.586	1.515	3229.37
6	145	2.0K	293.625	1.468	3077.84	4.617	1.522	3092.0
7	140	2.1K	297.5	1.4875	3057.6	4.586	1.515	3229.37
8	170	2.3K	395.25	1.976	2652.87	3.979	1.384	3227.8
9	180	1.9K	346.5	1.732	2833.58	2.106	0.898	1738.65
10	80	2.4K	194.0	0.97	3786.37	5.679	1.731	4207.67

Thus the worker number 2 having the maximum value of C_b and the minimum value R_b is likely to damage most devices. Workers 5 to 10 have the values as measured by Madzy[20] and it can be seen that in this case number 9 is most likely to induce maximum ESD damages.

Using Fig. 9.1 and the calculated values of 5 τ the P_{av}/A values can be estimated and then I_p and V_{ESD} values can also be calculated. The V_{ESD} values obtained from the graphical method will not be as accurate as in the previous case.

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10. ESD-PROTECTIVE MATERIAL SELECTION

Outline:

- Functions of ESD-protective materials
  * Low Triboelectric Generation
  * Dissipation of Static Charges
  * Shielding
  * Controlled Charge Bleed-off

  Material Characteristics
  * Volume Resistivity
  * Surface Resistivity
  * Decay Time

- Some Disadvantage of Using ESD-Protective Materials
  * Shedding
  * Corrosive Effect
  * Humidity Effect

- Application of ESD-Protective Materials
  * Antistatic Agents
  * Workbench Tops
  * Formed Shapes
  * Shunting Devices
  * Cushioning
  * Bags
  * Conductive Footwear
  * Flooring

- Requirements of Packaging Materials

- Other Desired Properties of ESD-Protective Packaging Material

- ESD-Protective Materials Testing

- Packaging Materials

- Attachments

The ESD-protected work areas provide primary protection to ESD-sensitive parts and assemblies during manufacture, test, packaging, maintenance, and other handling actions. The appropriate use of ESD-protective materials and grounding contributes a significant role in mimizing the buildup of electrostatic potentials. The areas of consideration for material selection include the floor types, floor polishes and cleaners, bench top materials, personnel shoes and clothing, carts, associated wheels and part carriers.

Functions of ESD-Protective Materials

In general, there are four basic functional characteristics of ESD-protective materials.

- Low Triboelectric Generation
- Dissipation of Static Charges
- Shielding
- Controlled Charge bleed-off.

Low Triboelectric Generation:

Electrostatic charges are generated by motion that is, rubbing and/or separation of materials. Triboelectric generation is the prime source of static charges. Every motion of a person or machine is a potential source of electrostatic charge. The contact and separation of shoes on the floor as they walk, and any relative movement of their clothing as they move, and any relative movement of materials or objects caused by their hands or by the machine are sources of electrostatic generation. Plastic is used for the packaging of electronic parts and assemblies are used due to their heatsealable characteristics, transparency, moisture resistance, and low cost. Plastic foams such as Styrofoam are widely used by manufacturers for reducing transportation shock and vibration without considering the damage to these part by electrostatic charges. Typical sources of electrostatic charges in production area are shown in Table 3.1.

There is no correlation between the resistivity and the ability of charge generation by the triboelectric effect. For example, aluminium, a highly conductive material, can generate substantial electrostatic charge when rubbed with other material whereby wood, although highly resistive, does not provide electrostatic charges. Plastic generates charges when rubbed with other materials. On the other hand, antistatic plastics, which are also relatively high in resistivity compared with plastics, do not generate charges. This may be due to the moisture absorption ability of antistatic material on the surface, which reduces friction and provides a conductive path for grounding of charges as they are generated during the rubbing motion. Therefore, the materials used for low triboelectric generation are bulk conductive and antistatic plastics, wood, composition wood, paper, cardboard, virgin cotton and some melamine laminates.

Dissipation of Static Charges:

This refers to materials with the ability to dissipate generated electrostatic charges. The conductive ESD-protective materials are defined as materials having surface resistivities of 10^5 ohm/$\square$ or less. Static dissipative materials are defined as those materials having surface resistivity between 10^5 and 10^9 ohm/$\square$. The materials are the same as conductive material, except the thicknesses are lower and volume resistivities are higher. Antistatic materials are defined as those materials having surface resistivities between 10^9 and 10^{14} ohm/$\square$. These include virgin cotton, wood and paper products. DOD-HDBK-263 provides a classification of materials based upon surface resistivity.

Shielding:

Two types of shielding are considered for ESD control.

Electrostatic field shielding or Faraday cage	–	Enclosing the object to be protected with materials having surface resistivity of 10^9 ohm/$\square$ or less.
EMI Shielding	–	For protection from EMI pulses caused by ESD spark discharge. EMI shielding requires highly conductive materials. With surface resistivity less than 10 ohm/$\square$

Controlled Charge Bleed-off:

When a good bonding is not provided between a charged source and ground, the discharge may take place in the form of a high-current discharge. This may result in a spark if the charge sink is highly conductive. In order to slow down the charges to an area to which a charged object is approaching (eg. a charged person's hand), highly resistive materials are used. Antistatic materials are best for this application. The ionization of air in the gap and the spark magnitude can be reduced as long as the time constant of the material is longer than the time in which the charged source approaches the material surface. The induced voltage will therefore drop along the material resistance instead of in air gap between the material and approaching charged object.

Decay Time:

This is an indirect method of measuring surface resistivity of a material. It is measured by charging a section of material with an electrostatic potential and measure the time for the voltage to decay to a given level see FED-STD-101B, method 4046 for detailed procedure). Materials whose surface resistivities vary with relative humidity, such as hygroscopic antistatic materials, will show variations in decay time at different relative humidities.

Some Disadvantages of Using ESD-Protective Materials:

Shedding:

The conductive particles, such as carbon particles as carriers for the conduction path of electrostic charges, used in ESD-protective materials can contaminate the clean room.

Corrosive effect:

The carbon-loaded foams contain chlorides and sulphides which can combine with moisture in the air to form hydrochloric and sulphuric acids. This will cause corrosion on the leads of integrated circuit package.

Humidity Effects:

Hygroscopic ESD-protective plastics provide surface conductivity by the formation of water on their surface. Therefore, the properties of these ESD-protective materials are a function of the relative humidity in the air. Hence, their effectiveness and the lower limit of relative humidity at which they should be used need to be evaluated.

Application of ESD-Protective Materials

Antistatic agents:

These can be used to minimize electrostatic charging due to triboelectric generation. Two forms are available, namely external (topical antistatic coating) and internal (additives) antistatic.

External antistatic material will reduce to ability of electrostatic charge generation and surface resistivity when it is applied to the surface of insulative materials. The external antistatic material consists of a carrier and an antistat. The carrier is the vehicle used to transport the antistat to a material, whereby the antistat is the substance that remains deposited on the surface of the material after the carrier has evaporated. They can be humidity dependent or non-humidity dependent. They reduce the electrostatic charge generation by increasing surface lubricity and surface conductivity. Their protection life time depends on the material to which they are applied, surface use and wear. Therefore, their effectiveness should be checked periodically.

Internal antistats are compounded into plastic during processing. They form a conductive path through the bulk of the plastics and bloom to the surface to absorpt the moisture from the air to dissipate electrostatic charges. Similarly, with external antistats these materials are also humidity dependent.

Workbench Tops:

The prime property of a workbench top should be low triboelectric generation of electrostatic charges. A secondary function of the workbench top is to dissipute static charges from charged ESD-sensitive items, or from persons touching the top in a slow controlled manner to prevent high current to or from the ESD - sensitive item and thus reduce sparking to a low level. Materials under selection should have low triboelectric generation capability and at the same time, have relatively high resistivity. Materials in the antistatic resistivity range meeting this criterial are wood, cellulose hard-board and melamine laminates etc. It is noted that the antistat can be removed from the surface by cleaning with freon, alcohol, and other hydrocarbon-based cleaners. Therefore, these materials should be cleaned with a topical antistat on a weekly basis.

Formed Shapes:

These refer to the form of assembly containers such as trays, shipping tubes, carriers, boxes, bottles, loaders and some hand tools etc. The materials used should have low triboelectric generation and electrostatic field shielding for most ESD - sensitive items and EMI shielding for sensitive memory devices. Metal containers such as aluminium without anodic coating provide the best protection, including shielding for electrostatic and EMI. Other conductive and static dissipative bulk conductive plastics also provide reasonable protection but not for antistatic materials which do not provide for statisfactory shielding protection. Therefore, antistatic containers should not be used for transporting ESD - sensitive items outside of protected areas without addition Faraday cage or EMI shielding.

Shunting Devices:

Low triboelectric generation and no shedding of particles are the main consideration for the shunting devices such as rigid clips, bars and forms. To be effective, the shunting devices should have a considerably lower resistance than the electrical circuit resistance between the leads or terminals to be protected.

Cushioning:

The materials used for cushioning foams and bubble packs for packing of ESD - sensitive items should have low triboelectric generation and provide good cushioning from shock, vibration, and handling. In addition, they should neither be corrosive nor affect solderability.

Bags:

The materials used for bags should have low triboelectric generation, provide against direct discharge through the bag, and shield the item from electrostatic field and EMI pulses. The bag should also be heat scalable, not react chemically, and not affect solderability of electrical leads of IC packages.

Conductive Footwear:

This is used in conjunction with conductive flooring to conduct charges from a person to the floor. Conductive heel grounders are made of a flexible band of carbon-impregnated polyolefin or polyethylene which covers the bottom of the heel of the shoe and tucks into the shoe to make contact with the person's foot.

Flooring:

ESD - protective flooring should be conductive and in the static - dissiputive resistivity range, and have the properties of low triboelectric generation and charge dissipation. ESD - protective floorings are in the form of carbon-loaded polyolefin, polyethylene, vinyl (sheet and tile squares), poured terazzo, and carpeting.

Requirements of Packaging Materials

The ESD - protective packaging should provide protection from the following listed potential hazards, incurred during transportation.

- Protection from physical damage to withstand vibration and shocks.
- Protection from Triboelectric Generation giving rise to the electrostic charge generation as a result of sliding, rubbing and separation of materials due to the shock and vibration of transportation and handling.
- Protection from Direct ESD to prevent discharge conducted directly from the outside through the packaging materials to the ESD - sensitive items.

This requires a layer of packaging which is able to provide adequate electrical resistance to the ESD - sensitive item without generating static from triboelectric effects such as Antistatic material.

- Protection from Electrostatic Field using a conductive bag during storage, transportation and handling.
- Protection from ESD - induced Sparks using in relatively conductive materials ($< 10\ \Omega / \square$) such as EMI shield.

Other Desired Properties of ESD - Protective Packaging Material

– Transparency.	Allows inspection and identification of packaged item without removing its protective covering.
– Heat sealability.	To ensure closure of the package for protection against contamination and humidity.
– Cleanability.	Resistance to solvent used in cleaning procedure.
– Resistance to sloughing.	To minimize the formation of particles of the packaging materials itself due to flexure or abrasion against the contained part.
– Toughners.	This property embraces flex resistance, tensile strength, fold endurance, and elongation, as well as impact strength.
– Solderability.	The material used for packaging should not emit gas or leave any residue on the electrical contacts that could result in poor solderability.

ESD - Protective Materials Testing

Below is a summary of standard test procedures for measuring resistivities of conductive, static dissiputive, and antistatic materials:

1. American Society for Testing and Materials procedures for conductive materials, ASTM D991–75.
2. American Society for Testing and Materials procedure for static dissipative, antistatic, and insulating materials, ANSI/ASTM D257–76.
3. Federal Test Method Standard for measuring electrostatic decay time, FED–STD–101B, Method 4046.

4. American Society for Testing and Materials tests for measuring the electrical resistance of conductive flooring, ANSI/ASTM F150–72 (1979).

5. American Association of Textile Chemists and Colorists test method for the measurement of the electrostatic property of carpets, AATCC 134 (1979).

6. National Fire Protection Association standard for electrical resistance measurement of conductive flooring, NFPA No. 56A (1978).

Packaging Materials

- Carbon-Impregenated Polyethylene or Nylon.

- Antistatic Polyethylene or Nylon (transparent).

- Aluminized Laminates. It consists of an outer layer of metallized spun-bonded polyolefin, a middle layer of aluminum foil, and an inner layer of black carbon-leaded polyethylene. However, this material is not conductive. It has good moisture resistance characteristic and provides EMI/electrostatic field shielding, but will generate charges on the polyethylene surface.

- Cellulose – Based Materials.

- Hybrid Laminates. Materials have been developed for use as an insulative intimate surface to prevent ESD through the material. A conductive lamination on the outer surface provides protection against EMI/electrostatic field.

- Open Cell and Plastic Foams. Used for cushioning purposes (antistatic and conductive).

11. IDENTIFICATION OF EOS/ESD IC FAILURE

OUTLINE

- ESD Susceptibility of ICs
- Sources of EOS
- ESD/EOS Failure Modes in MOS Devices
- Understanding of Basic Failure Mechanisms
  * Junction Breakdown
  * Oxide Repture
  * Metallisation Burnout
- ESD/EOS Failure Examples
  * CMOS IC
  * Operational Amplifier
  * Power IC for Automobiles
- Consideration of Time-Dependent ESD Failure
- Systematic Approach in Failure Analysis of ESD/EOS – Induced Failure
  * Gather Information
  * Plan Analysis Strategy
  * Failure Modeling
  * Fault Isolation and Mechanism Determination
  * Develop Corrective Action
- Electrical characterization of ESD/EOS Failure
- Decapsulation of ICs
- Layer Stripping Processes
- Isolation of Invisible ESD/EOS Damage
  * Photoemission
  * EBIC
  * IR Microscopy
  * Liquid Crystal Hot Spot Detection
- Failure Verification By Decoration
- EOS or ESD: Can Failure Analysis Tell The Difference?
- ESD In IC Assembly

ESD Susceptibility of ICs

The advancing trend of technology towards smaller circuitry dimensions and hence a thinner gate oxide dielectric layer has prompted for a higher device ESD susceptibility level, specially in MOS technology.

In general, ESD failures can occur in different ways as summaried below:

- Direct. These are failures which result from direct contact of the IC with a substantial electrostatic charge causing breakdown in the device.

- Latent. These are failures which occur via degradation of the devices over a period of time. The time dependency of device failure may suggest a cummulative effect of charges, by which an IC being subjected to repeated exposure of ESD at a lower static potential would cause direct failure.

Regardless to the type of mechanism; the device failure is either power sensitive or voltage sensitive. Voltage sensitive parts fail due to dielectric breakdown of dielectric layers, while power sensitive devices fail due to thermal breakdown.

Integrated circuit failures caused by ESD are attributed by one of four models. The first is known as the Human Body Model and consists of a lumped element capacitor and series resistor to simulate the human body parameters. In this model, the human body is charged triboelectrically, ie, by walking across a floor, rubbing on some plastics, etc., and then discharged to a device by direct contact. Energies in the millijoule range are discharged with microsecond time constants that cause heating of junctions, resulting in parametrics shifts or complete device failure.

The second model is concerned with an electrostatic induced fields. A device under a high electrostatic field can have a potential induced across some oxide areas. Under contain conditions of device structure orientation, the induced field may exceed the dielectric strength of the oxide and cause heat breakdown.

The third model is a of charged device discharging to ground. Electrostatic charges may buildup on devices during handling, shipping and packing due to the triboelectric effect. If one pin from a charged device is grounded, a current pulse can flow through the device which may be capable, depending on the size and duration of the pulse, of damaging or degrading the chip.

The fourth is the Machine Model and it can cause damage to the devices at a lower voltage level compared with the Human Body Model. The industry accepted standard for the Human and Machine Models are as listed below:

Model	*Capacitor*	*Resistor*
Human	100 pF	1500 ohms
Machine	200 pF	0 ohms

The series resistor in the Human model tends to "SOFTEN" the pulse rise time at the IC inputs which allows the protection circuit time to react and discharge before it can cause damage. The charge developed in the Machine model is much more destructive as it has a very abrupt rise time that can damage the input protection circuit at much lower voltage (typically 3 or 4 times lower than Human Model survival voltage).

Sources of EOS

Electrical Overstress (EOS) is normally generated from ignitors as in automobiles, inductive loads in electric motors and high voltage generators such as colour TV sets etc., in the form of high sinking currents seen at the device output pins discharged either to ground or power pins.

EOS/ESD Failure Modes in MOS Devices

There are a number of failure mechanisms associated with MOS devices and VLSI circuits related to overstress conditions. The failure modes can be attributed to thermal breakdown, gate oxide breakdown and latch-up. The device failure due to junction breakdown may result in a reduction of reverse breakdown voltage and increase in leakage currents. For metal traces, metal opens or shorts and electromigration are commonly observed. The oxide breakdown is another major failure mechanism which has reached a higher susceptibility level due to scaling of gate oxide thickness to lower values.

Understanding of Basic Failure Mechanisms

Three mechanisms can be identified for semiconductor devices subject to ESD/EOS. They are junction breakdown, oxide rupture and metallization burnout.

Junction breakdown is usually associated with bipolar discrete and integrated circuits while oxide rupture is associated with MOS devices. Metallization burnout is seen in most of the devices.

Junction Breakdown:

P-N junction breakdown is due to the injection of an electrical transient of sufficient magnitude and duration to initiate second breakdown and subsequently to melt the junction. For example, when a constant voltage is applied to the semiconductor junction, power is dissipated which causes the temperature of the junction to rise. Hot spots will form due to current constrictions caused by geometry and inhomogenieties in the junction. Eventually, the silicon in the hot spot will display instrinsic behaviour, leading to a negative coefficient of resistance. Thus, as the temperature continues to rise, current will be shunted into the hot spot, resulting in thermal runaway. The thermal runaway will cause the silicon in the hot spot to melt, thus shorting the junction.

It is generally easier to destroy reverse biased junctions than a forward biased one due to the power dissipated in the depletion region of the reverse biased junction. The current needed to burnout the forward biased junctions is in the order of 5 to 15 times greater than that needed for a reverse biased junction. The emitter-base junction is usually the most susceptible in diffused transistors since it is the smallest, and hence subjected to higher power densities. With increasing circuit densities, integrated circuit junctions have become smaller, leading to greater susceptibility to ESD/EOS.

Oxide Rupture:

This is referred to as gate oxide shorted to the substnate. This occurs when the voltage applied across the gate has sufficient magnitude to cause breakdown, allowing current to pass. Once the oxide has brokendown, it requires very little extra energy to destroy the oxide, which results in a short circuit. Because of this, the gate oxide short circuit occurs almost immediately after the application of ESD. This failure mechanism makes MOS devices very susceptible to ESD since the breakdown voltage for oxide is less than 50 voltage for oxide thickness of 500 Angstrong.

Because of this problem, an input protection circuit is added to IC chips during design. Thus, the failure site on MOS ICs may no longer be the gate oxide of the input invertor only, but the protection diode itself.

Metallisation Burnout:

This occurs upon the injection of a current pulse of sufficient magnitude and duration to melt the metallisation trace through Joule heating. This type of damage is normally observed as an open circuit in the device. Metallisation burnout is frequently a secondary failure mechanism. This occurs when at secondary breakdown, a gate oxide rupture results in a short circuit which then drains enough current to melt the metallisation. In this case, the junction or oxide fails first, with the metallisation burnout occuring after the device has failed. As the circuit densities increase, the metallisation traces become smaller, leading to a higher susceptibility to ESD/EOS.

ESD/EOS Failure Examples

CMOS IC:

The device is designed with build-in input protection network to prevent ESD. The input protection circuit consist of a series resistor, and diode(s), which are placed in parallel with the input. When the overvoltage, which is developed across the protection diode(s) exceeding its reverse breakdown voltage, is applied to the input, the excess current flows through it from the input to ground. While the excess current flows through the diode and the resistor, Joule heating causes this portion to be damaged. Typical failure modes of MOS IC are the degradation of I-V diode characteristics or a resistive short circuit between the input and ground. Microscopic inspection of the surface surrounding a damaged junction will show no obvious damage.

Operational Amplifier:

The pair of differential input transistors of an operational amplifier are susceptible to severe damage from ESD/EOS. Electrical tests of failed devices show latch up of the output voltage, a very high input offset voltage and a low gain. Curve tracer tests revealed the degradation of I-V characteristics between the two differential input terminals. Visual inspection of the failed sample which exhibited latch up of the output voltage showed a flash over on the surface of the base-emitter junction.

Power IC for an automobile:

Failed power IC from field return is observed to have a resistive short between the power supply (Vcc) and the output pins or the output pin and the ground, or open circuits at output pins. Visual inspection of the defective part after decapsulation had shown burned or open metallisation. The p-n junctions of single ended push-pull output transistors were catastrophic damaged. This failure was due to the secondary breakdown of the output transistor, when the single pulse applied to the ground pin exceeded the safe operating limit for the output transistor.

Consideration of Time-Dependent ESD Failure

For MOS structure there is a basic premise that an exposure to ESD might result in very subtle damage to gate oxide resulting in little or no gate oxide rupture. This degraded oxide may later fail at a much lower voltage threshold that occurs in use conditions. It is also possible that a rather severely resistive shorted gate oxide might improve either during the initial or subsequent static exposure. It is also possible to damage the protection diode(s) by ESD resulting in "softened" I-V reverse biase characteristic of questionable reliability, but still within the device specification. It is also possible that a high voltage single surge occuring during discharge may result in a disruption of the charge equilibrium of a device. This could lead to accumulated charges on the devices surface or in the gate oxide.

P-N junction degradation induced by ESD usually results in a softened I-V reverse bias diode characteristic. This is due to the locallized heating during the transient and resultant filamentation that shunts the p-n junction. The device may be further degraded during use.

Aluminium and silicon transport mechanisms resulting in alloying and eventual short circuits generally occur at high temperature. Yet it is conceivable that a filament across a p-n junction might be of such an effective cross-section to cause further locallized heating in life resulting in higher leakage and eventual failure. It is also possible that a severely degraded junction can be improved through subsequent exposure to ESD. However, such a degraded junction may easily fail in use.

Sites of constriction in metal traces have been known to fail due to ESD. It is possible that ESD could further reduce the cross-sectional area of such a site. This type of metal trace could fail in the field due to electromigration.

Systematic Approach in Failure Annalysis of ESD/EOS – Induced Failure

ESD/EOS failure analysis is not just about techniques. Equally important is a disciplined procedure for a systematic application of physical analysis techniques. Failure Analysis is a problem-solving tool where the problem has to be defined precisely, resulting in an unmistakable cause of failure. The methodology for analysing ESD/EOS – Induced failure can be divided into five stages:

- GATHER information
- PLAN analysis strategy
- failure MODELING
- fault ISOLATION and mechanism determination
- DEVELOP correction actions.

Gather Information:

a. Define nature of the problem

b. Identify source of failure (where, when and how etc.)

Plan Analysis Strategy:

a. Define analysis techniques needed for identifying suspected failure mechanism.

b. Determine the sample size of defective parts for analysis.

c. Plan analysis steps

d. Estimate time of completion and establish time points.

Failure Modeling:

a. Characterize anomalous behaviour or appearance.

b. Review analysis data to localize failure.

c. Develop a preliminary theoretical model for failure and propose physical cause(s).

Fault Isolation and Mechanism Determination:

a. Isolate proper operating regions from inproper operating regions using analytical techniques.

b. Characterize anomalous behaviour at (isolated) failing location.

c. Verify the failure model with additional or simulated experiment(s).

d. Propose a failure mechanism.

Develop Corrective Action:

a. Project the possible cause.

b. Propose corrective actions to eliminate failure.

Electrical Characterization of ESD/EOS Failure

The device is characterized by the following approaches:

A. Sweep the voltage across the device pin in a powered up configuration. This will enable the detection of the gate oxide damage at the input invertor, as would be caused by a short surge and the input protection diode(s) not responding fast enough to clamp the voltage. The I-V characteristic obtained with this arrangement is the forward bias characteristics of two input protection diodes at different voltage polarities.

B. Sweep the voltage at the input or I/O pin with respect to Vss or ground to obtain the I-V characteristic.

Decapsulation of ICs

Decapsulation is a technique, either chemically or mechanically, to remove the plastic mould compound to expose the surface of Integrated Circuit for microscopic examination.

Technique	*Description*
Dropper	Nitrid Acid (99%) with the unit heated up to 150 degree C.
Submersion	Hot sulphuric Acid (97%) at 285 degree C.
Mechanical	Cutting pliers
Spray Etch	Jet etch machine with hot concentrated Sulphuric Acid at 285 degree C.

Layer Stripping Processes

Chemical etching is a layer stripping technique. The chemical process of etching proceeds generally in two phases. The first is an Oxidation-Reduction reaction in which the semiconductor is promoted from the zero oxidation state to some higher oxidation state. The oxidation reaction requires holes for its execution, while the reduction reaction requires electrons (and occurs simultaneously with the oxidation), is accomplished by the liberation of holes. The second reaction involves the dissolution of oxidation products in the form of complex soluble ions. This is done by means of complexing agents. The alternative method of the wet etch technique is the dry etch technique.

Layers To Be Removed	*Technique*
Passivation	H_3PO_4 : H_2O
Metallisation	Aluminium etch
Poly silicon	200 CH_3COOH : 80 HNO_3 : 1 HF

Isolation of Invisible EOS/ESD Damage

The transistors that have been degraded by ESD/EOS often have no visible internal damage. Photo emission electron beam induced current, IR Microscopy and Liquid Crystal are useful fault isolation techniques in locating ESD/EOS failure site. The subsequent chemical staining techniques will make the damage visible.

Photoemission:

When emitter-base junctions are reverse-biased into breakdown, they tend to emit light at the junction. This light results from the emission of photons, which account for the loss of energy following the recombination of electrons and holes at the junction. If there is a site in the junction where localized early breakdown is occuring, light may be emitted from that area, at a voltage below those at which light becomes visible otherwise. In failure analysis, the junction is observed under a microscope with very low illumination while the reverse voltage is slowly increased. Areas where light is first seen are noted for attention during subsequent analysis.

EBIC:

In the EBIC mode of Scanning Electron Microscope (SEM) operation, hole-electron pairs that are generated in a semiconductor by the beam create current are collected and used to form an image. When connected and adjusted properly, the contrast observed delineates the semiconductor junctions and irregularities in them.

IR Microscopy:

Large amounts of current may flow for the device having ESD/EOS failure. Given the proper current densities, under forward bias conditions most semiconductors will emit light whose wavelength depends upon the band gap of the material. In silicon, such emission occurs at a wavelength of approximately 1.1 m – Infa-Red (IR) Region.

The radiation can be detected by means of IR Microscopy at the device level, and the failure site can be isolated. The observation is not thermal emission, but rather, of IR radiation resulting from the recombination of holes and electrons at the failure site.

Liquid Crystal Hot Spot Detection:

This technique uses cholesteric liquid crystals and polarized light to locate areas of high power dissipation on an integrated circuit. A thin layer of a cholesteric liquid crystal appears transparent when viewed through a polarizing microscope (microscope with perpendicular polarizers placed in the optical path, positioned between the object & eyepiece). If a portion of the IC is sufficiently heated due to excessive leakage current, so that liquid crystal material charges from cholesteric phase to isotropic (true liquid) phase, the polarized light in this area will not be rotated, which, therefore, appears as a dark spot under observation.

Failure Verification by Decoration

The wet staining technique is used to verify and examine the isolated failure site by photo-emission or EBIC. The passivation layer, aluminium metallization and insulating/dielectric layer are removed using standard Dry or Wet etching techniques. High manification by optical microscopic examination after layer removal may observe some surface anomalies that were suspected by ESD/EOS damage. However, in most cases these are either extremely subtle or virtually invisible. Etching into the silicon itself may be much more rewarding.

At room temperature, the following formula is applied for staining.

1 part by volume HNO_3 (70%)
3 parts by volume HF (49%)
10 parts by volume CH_3COOH (99.7% glacial)

This etch removes more highly doped silicon at a faster rate. When it is applied to the IC chip, it creates a physical step in the emitter/base junction and holes in the areas where aluminum alloying (if any) has occured.

EOS or ESD: Can Failure Analysis Tell The Difference?

Electrical overstress (EOS) and electrostatic discharge (ESD) as causes for semiconductor IC failure are difficult to differentiate. Physical analysis alone cannot provide complete information on the full range of factors affecting device failure and it is only part of investigation process. To make the distinction, it is essential to correlate the physical analysis data with engineering, testing and reliability.

ESD In IC Assembly

Major sources of electrostatic generation occur anywhere in an IC assembly process from the most innocent handling procedure to the most complex automatic equipment.

Problem	*Solution*
1. Teflon spin drying racks (8 kv).	1. Stainless steel spin dry racks.
2. Some ungrounded operators (10 kv).	2. Ground all operators.
3. Some ungrounded table tops (5 kv).	3. Ground all handling tables.
4. Glass beakers, dishes and slides (4 kv).	4. Stainless steel beakers.
5. Chip trays (6 kv).	5. Carbon filled chip trays.
6. Wafer boxes (5 kv).	6. Carbon filled wafer boxes.
7. Plastic storage cabinets (10 kv).	7. Faraday cage storage.
8. Plastic vacuum chip pick up (1.5 kv).	8. Transparent Ni coated vacuum tips.
9. Rubber chemical gloves (3 kv).	9. Conductive gloves.
10. Finger cots (0.5 kv).	10. Antistatic finger cots.
11. Wafer break papers (2 kv).	11. Aluminum coated wafer break papers.
12. Personal clothing (30 kv).	12. Conductive Smocks.

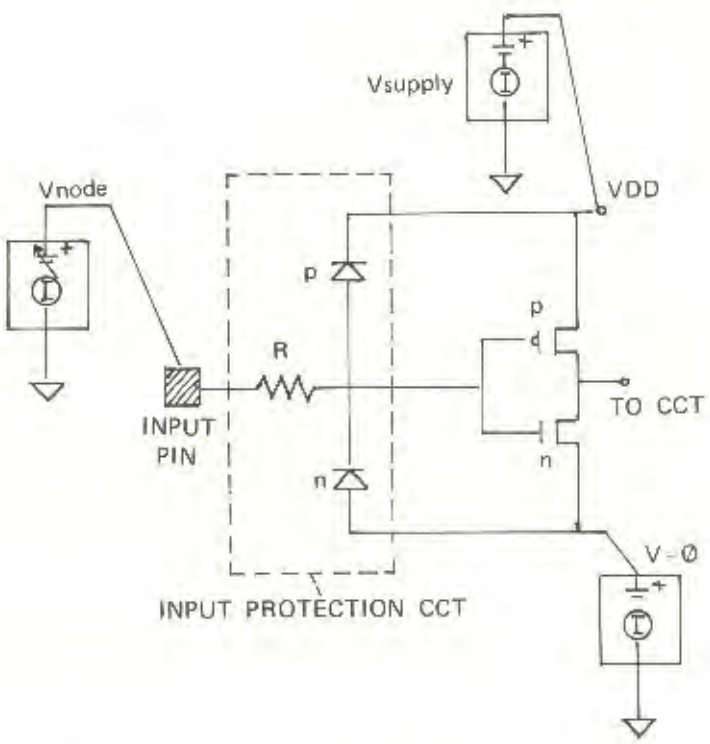
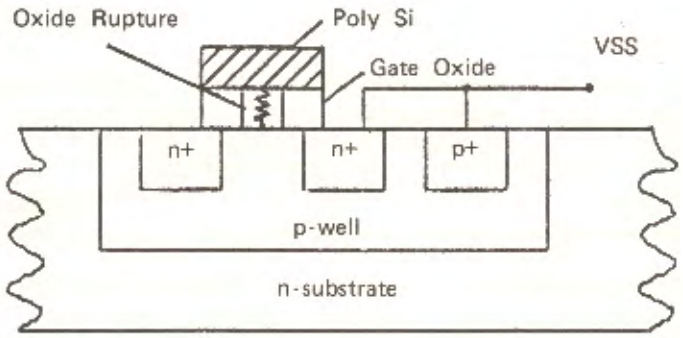
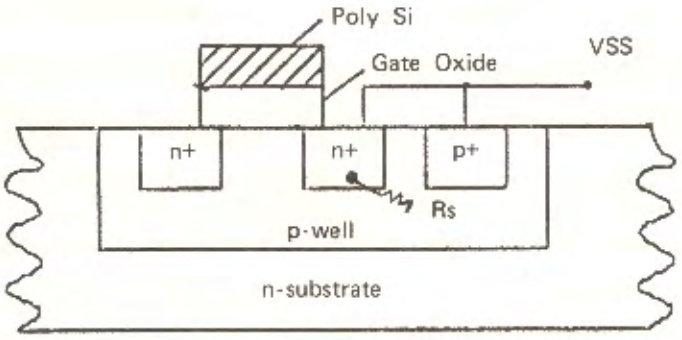


Fig. 11.1 – The set up of Device pin electrical characterisation with power up configuration.





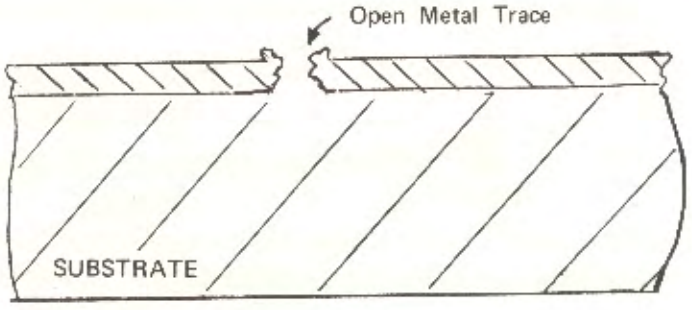


Fig. 11.2 – Failure Mechanisms associate with ESD/EOS

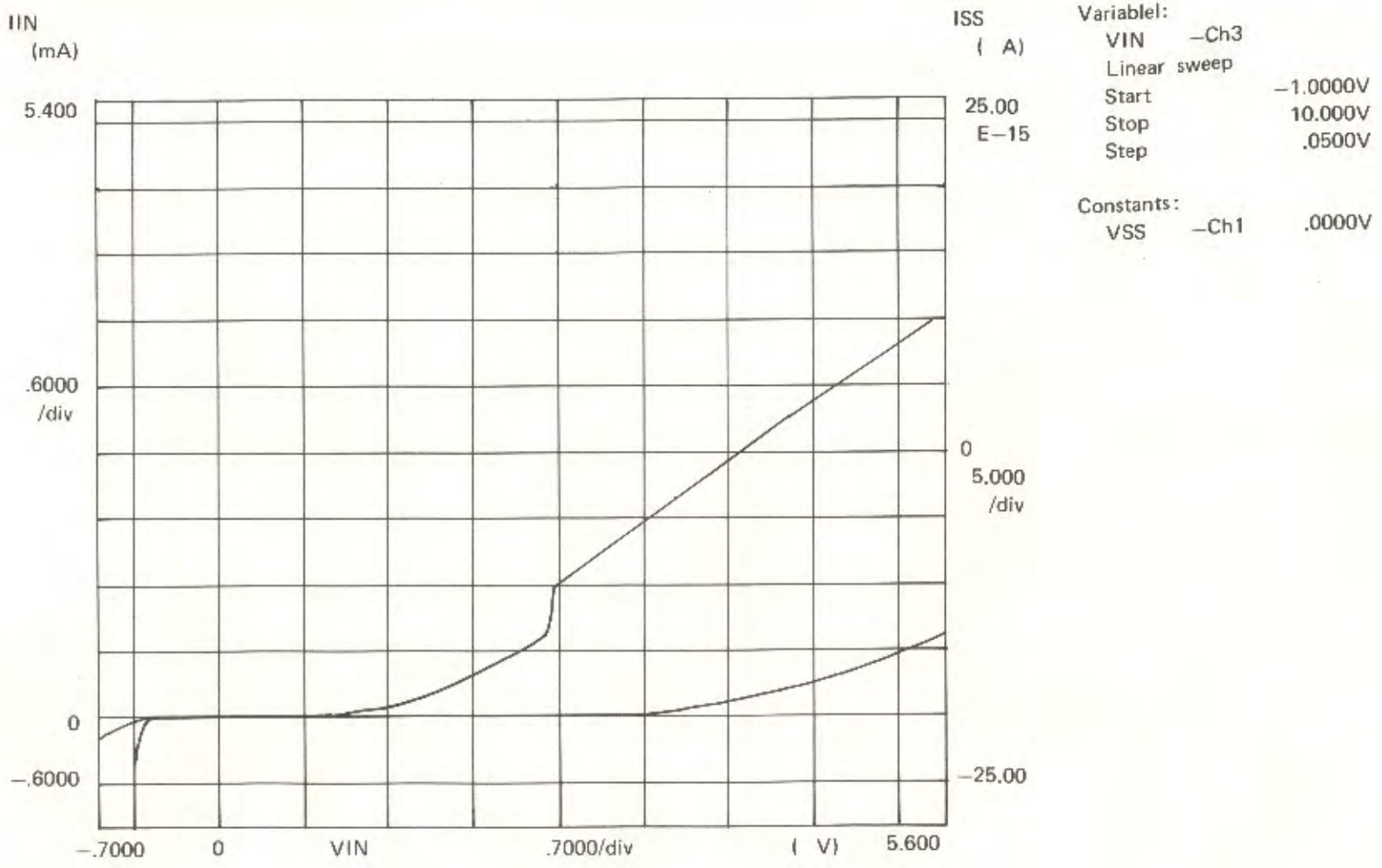


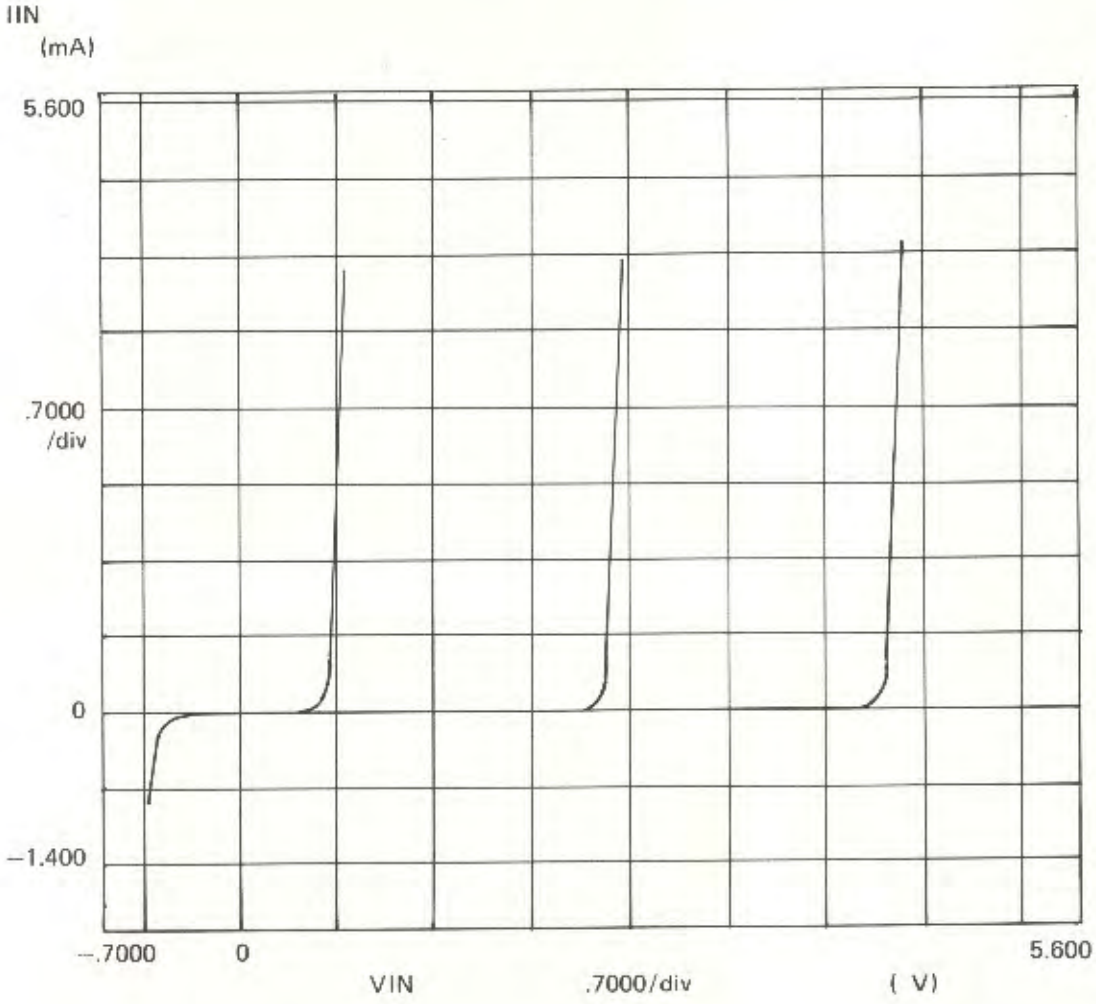
FIG. 11.3 — JUNCTION DEGRADATION

Variable1:
VIN —Ch3
Linear sweep
Start —1.0000V
Stop 10.000V
Step .0500V

Constants:
VSS —Ch1 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE 1	15. 0E—03	66. 5E+00	13. 2E—03	—198E—06
LINE 2				

FIG. 11.4 – RESISTIVE SHORT

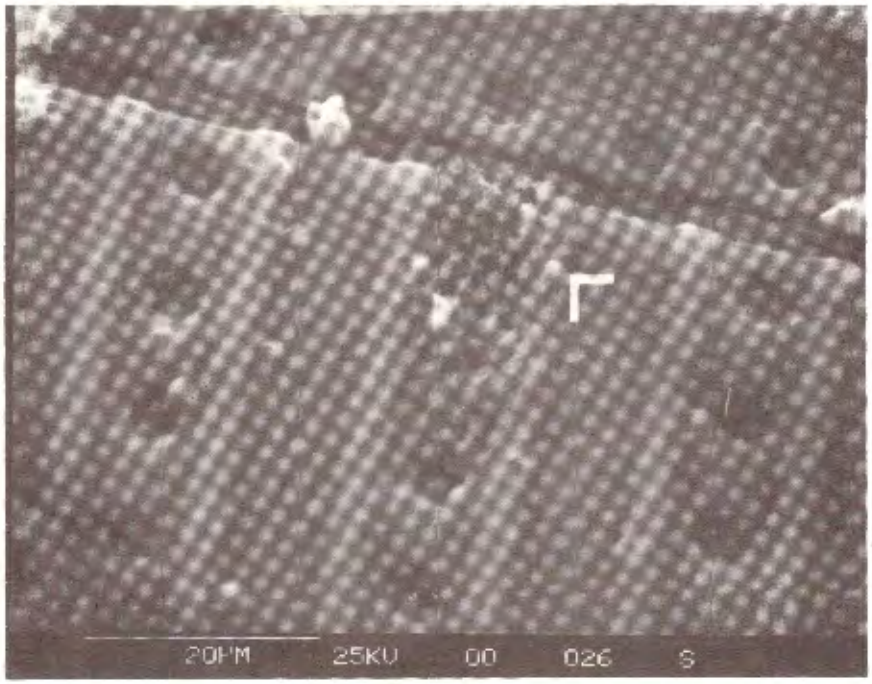


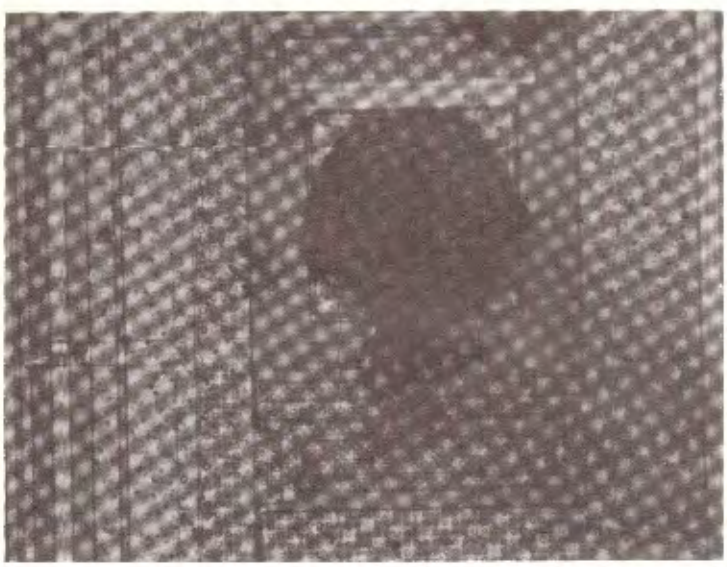
Variable1:
VIN —Ch3
Linear sweep
Start −1.0000V
Stop 6.0000V
Step .0500V

Variable2:
VDD —Ch4
Start .0000V
Stop 4.0000V
Step 2.0000V

Constants:
VSS —Ch1 .0000V

FIG. 11.5 — I/P VS 0, 2, 4V BIAS





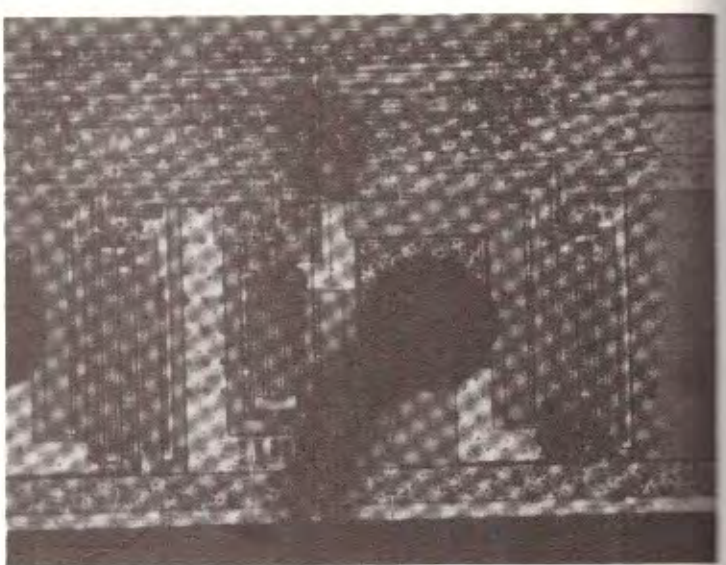
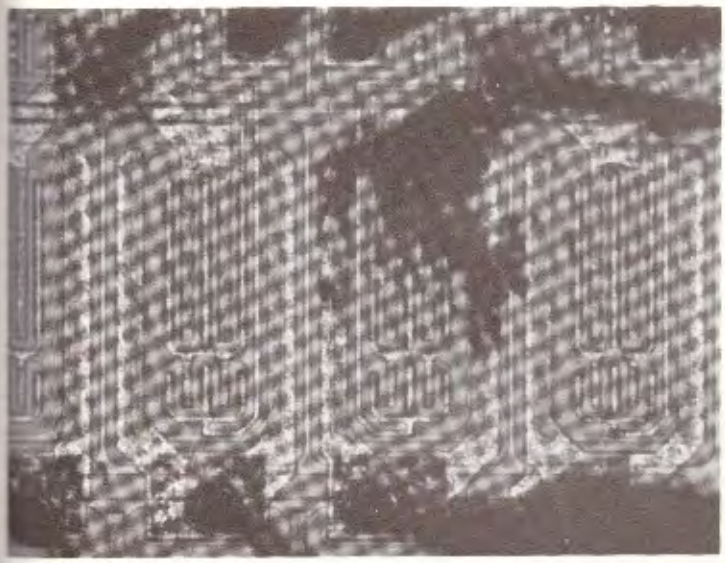
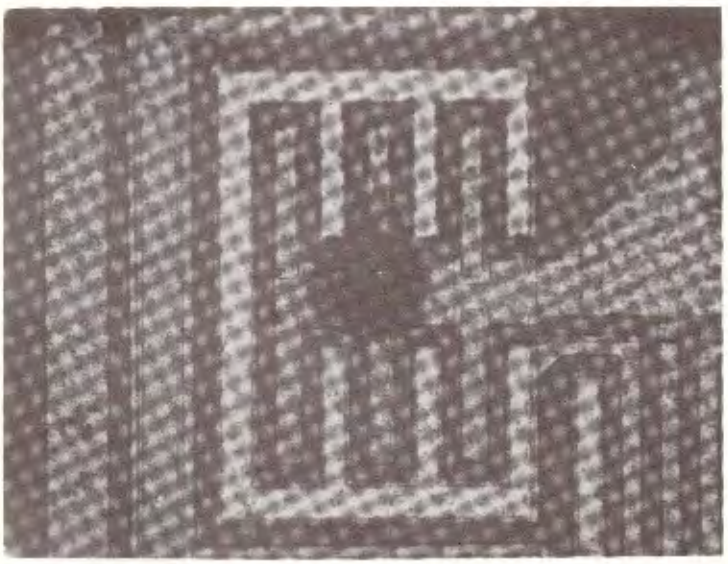


FIG. 11.6 – EXAMPLES OF ESD FAILURES





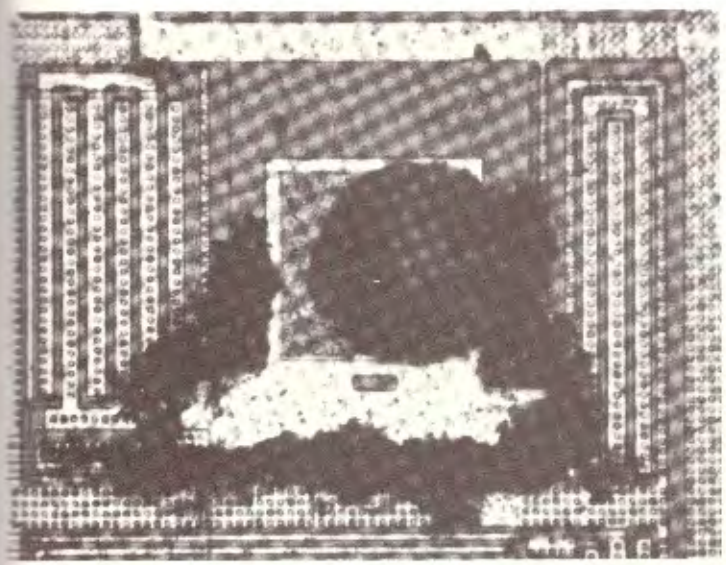


FIG. 11.6 – EXAMPLES OF ESD FAILURES (CONT.)

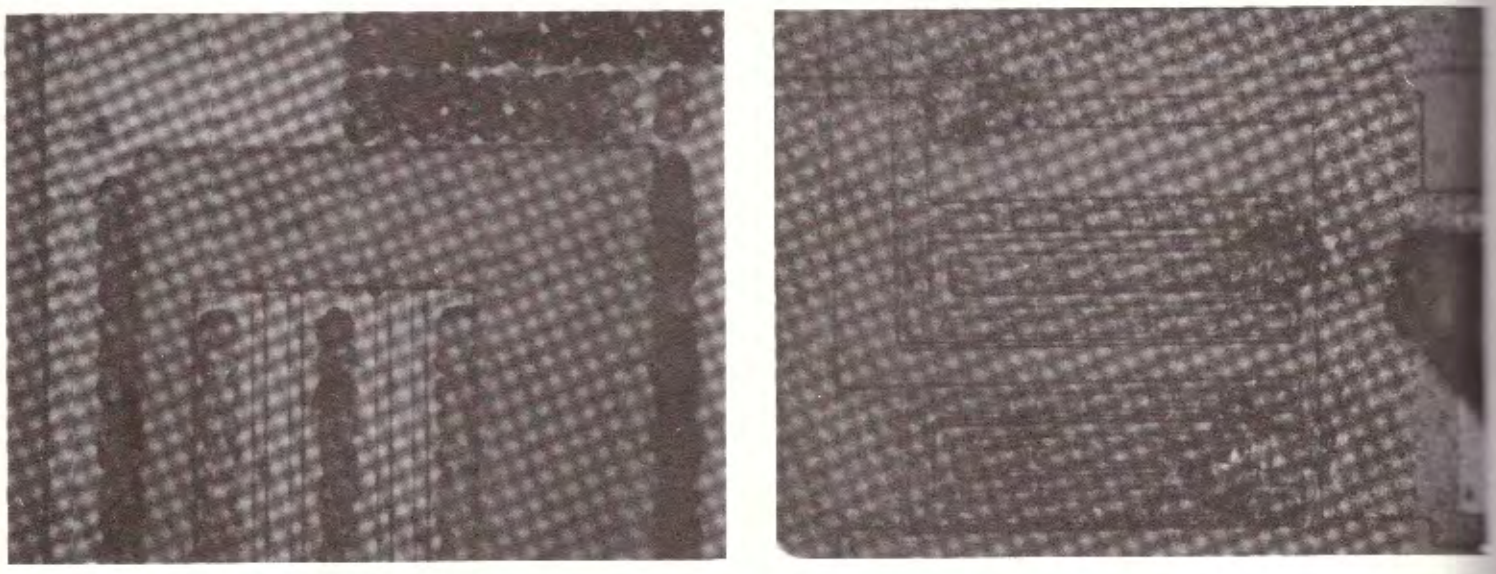


FIG. 11.6 EXAMPLES OF ESD FAILURES

12. ESD STANDARDS

INTRODUCTION

The awareness of Electrostatic discharge problems in the semiconductor and Electronics industries opened new fields and opportunities in this manufacturing sector. There is a flood of information on ESD from materials to implementation programs, equipments and procedures. With the flood of information, there is a new problem of conflicting or superfluous or confusing recommendations that standardisation is badly needed.

There are various standards related to ESD. For the semiconductor and electronics industry, the most well known are the following:

DOD-STD-1686	—	Electrostatic Discharge Control program for protection of electrical and electronic parts, assemblies and equipment.
DOD-HDBK-263	—	Electrostatic Discharge Control handbook for protection of Electrical and Electronic parts, assemblies and equipment.

Other associated specifications related to semiconductor and electronics components are as follows:

MIL-M-38510	—	General Specifications for microelectronics.
MIL-STD-883	—	Test Methods and procedures for microelectronics.
MIL-M-55565	—	Packaging of microcircuits.
MIL-STD-129	—	Marking for shipment and storage.
MIL-STD-1285	—	Marking of electrical and electronic parts.

SCOPE OF IMPLEMENTATION

The implementation of ESD program in a factory is often confusing in the scope of implementation. This confusion arise due to lack of knowledge of the necessity to implement the ESD program or confusion between necessity and desirability.

A manufacturer (component manufacturer or user) will have to understand what he means by the necessity to have an ESD program. Two viewpoints need to be considered necessary which are: those required by specification and those required technically so that the losses due to ESD can be minimised. Outside of these considerations will be considered as what is desirable but not necessary.

The major specifications on ESD do not explicitly spell out the scope of implementation in a manufacturing facility but requires the program to cover by product types: components, assemblies and equipments. The scope of ESD control program required in manufacturing plants is spelled out in the relevant component specifications such as MIL-M-38510 for microcircuits (or MIL-S-19500 for semiconductors).

In the MIL-M-38510, the ESD handling precautions for microcircuit devices need to be exercised from lead clip or wire bond (for packages which do not have shorting bar or do not have leads shorted together). An extract of this requirement from paragraph 4.4.2.8 of this military standard read as follows:

4.4.2.8 Electrostatic discharge sensitivity. Electrostatic discharge sensitivity testing shall be done in accordance with method 3015 of MIL-STD-883, and the applicable detailed specification (see 3.6.9.2). Devices found to be sensitive to ESD shall be handled in accordance with the manufacturers in-house control documentation. Handling shall begin at lead clip or wire bond (i.e., for packages which do not have lead shorting bar, or do not have leads shorted together).

Handling documentation shall be submitted for approval to the qualifying activity. A model ESD control program is available upon request from the qualifying activity and may be used as a guideline document.

Do note that the military standards specify only the minimum requirement as a general statement. However, one must consider the technical consideration and sensitivities of each device to ESD. There have been many papers and industrial experimentations to show that even before the wire bond operations devices are still susceptible to ESD. One must understand the qualitative physics of ESD in damaging devices. The damage comes about when there are significant potential differences between 2 layers in the microcircuit or semiconductor. What is "significant potential difference" varies from devices to device and the quantitative determination of this significant potential difference is what we would term as device susceptibility level.

The other desirables are related to implementations to ensure consistency and manufacturing discipline, there are possible but unproven or unexplained potential damages, as such there are even vendors or customers who insist that the ESD program should extend to devices which have shorting bars.

What is most important in understanding the scope is to differentiate and understand the "necessities" versus "desirable" to draw up and implement a cost effect ESD Control program.

Definitions

There are various terminologies that need to be defined first before further discussions on the ESD Control program. These are:

1. *Antistatic* – An antistatic material resist tribo-electric charging upon contact and separation with another material. Plastic materials impregnated with antistatic agents (antistats) are antistatic if their surface resistivity is between 10^9 and 10^{14} ohm/square.

2. *Conductive* – A conductive material is one capable of electrostatic field shielding and having a volume resistivity of 10^3 ohm-cm maximum or a surface resistivity less than 10^5 ohm/square.

3. *Static Dissipative* – ESD protective materials having surface resistivities greater than 10^5 but not greater than 10^9 ohm per square.

4. *Insulating* – An insulating material is defined as having a volume resistivity of 10^{12} ohm-cm minimum or a surface resistivity of 10^{14} ohm/square minimum.

5. *Decay Time* – The time for a static charge to be reduced to a given percent of the charge's peak voltage.

6. *ESD protective material* – Material capable of one or more of the following: limiting the generation of static electricity, rapidly dissipating electrostatic charges over its surface or volume, or providing shielding from ESD spark discharge or electrostatic fields.

7. *ESD protective packaging* – Packaging with ESD protective materials to prevent ESD damage to ESDS items.

8. *ESD Sensitive (ESDS) Items* – Electrical and Electronic parts, assemblies and equipments that are sensitive to ESD Voltages of 15000 Volts or less.

9. *Electrostatic field* – A voltage gradient between an electrostatically charged surface and another surface of different electrostatic potential.

10. Ground – A mass such as earth, a ship or vehicle hull, capable of supplying or accepting large electrical charge.

11. *Protected Area* – An area which is constructed and equipped with the necessary ESD protective materials and equipments to limit ESD voltage below the sensitivity level of ESDS item handled herein.

12. *Protective handling* – Handling of ESDS items in a manner to prevent damage from ESD.

REQUIREMENTS RELATED TO DEVICE HANDLING

Handling is defined as actions in which items are hand manipulated or machine processed during actions such as inspections, manufacturing, assembling, processing, testing, repairing, reworking, maintaining, installing, transporting, failure analysis, wrapping, packaging, marking or labelling.

For microcircuits, the device handling requirements are spelled out in the military microcircuits specification, MIL-M-38510 and associated documents listed in the applicable documents section, which included, MIL-M-55565, MIL-STD-129 and MIL-STD-883.

Note that in these four standards, the relevant references to ESD are related to device preparations for shipment, i.e. device marking, packing, shipping and susceptibility tests.

There is no explicit reference in the military standards invoking the use of DOD-STD-1686 or DOD-HDBK-263.

Thus, in this section, I will dwell only on requirements spell out in the four standards mentioned for microcircuits.

Device Marking

In the MIL-M-38510, the ESDS identifier is required to be marked on the top of the package. Paragraph 3.6.9. and 3.6.9.2. allows 3 options to be marked on the device:

a. MIL-STD-1285 Sensitive Electronic device Symbol.

or b. Outline of equilateral triangle (i.e., $\triangle$).

or c. Color code conforming to FED-STD-595.

Such devices are classified as category A and manufacturers may opt for this category without performing ESD sensitivity test based on their own history, judgement or performance.

Devices which are not marked with ESDS identifier are classified as category B, and require to be tested for ESD sensitivity to verify that classification is correct.

In paragraph 3.6.10, the device carriers such as unit carriers, unit pack (i.e. individual foil bag) unit container (e.g. Faraday shield), and multiple carriers (e.g. tube, rail, magazine) for delivery shall be marked according to MIL-STD-129 and MIL-M-55565 for ESDS microcircuits.

In MIL-M-55565, the material types for carriers, wrapping and cushioning for packing of microcircuits require antistatic as a minimum and should be protected from ESD during handling, shipment, storage from time of manufacture to point of use. This is accomplished by use of heat sealed bags fabricated from one continuous piece.

In MIL-STD-1285, marking on unit package of ESDS items is needed if unit size precludes the marking. This marking is as follows:

Device Packing

In MIL-M-38510 para 5.1, requires packaging to be in accordance to MIL-M-55565. ESDS devices (category A) are required to be packed in conductive material or in antistatic material with an external conductive field shielding barrier. Coated antistatic rails is allowed to be used once only unless the antistatic property is proven to be intact on the surface.

Examples of acceptable packaging are:

a. Unit container consists of 3 layers with an inner antistatic surface and one of the following options: Electrostatic field shielding exterior layer and an insulative intermediate layer or an insulative exterior layer and a conductive electrostatic field shielding intermediate layer.

or

b. Conductive non-corrosive rail with non-corrosive and conductive or antistatic foam plugs at both ends of each rail to prevent movement

or

c. Antistatic non-corrosive rails with non-corrosive and conductive or antistatic foam plugs both ends of each rail to prevent movement. Antistatic rails shall be packaged in conductive, electrostatic field shielding material.

ESD Handling Control Program

In the MIL-M-38510, this requirement is generally spelled out in Appendix A para 20.1.1.14 which is as follows:

20.1.1.14 The ESD handling Control program documentation shall be under document control. This includes methods, equipments and materials, training, packaging, handling and procedures for handling ESDS devices.

This standard does not provide details of adequate ESD Handling program. Thus for purposes of understanding ESD and to provide a minimum guideline, DOD-STD-1686 for ESDS items upto 4000 Volts and DOD-HDB-263 for device susceptibility exceeding 4000 Volts have been generated.

In this section, these 2 documentations are being discussed. There is confusion if one were to read the 2 specifications and wonder why there are 2 such documentations.

DOD-STD-1686 Versus DOD-HDBK-263

There are two major differences in the 2 documents, which are:

SCOPE AND PRESENTATION

DOD-STD-1686 is intended for parts sensitive to 4000 Volts (para 1.1 of this standard) while DOD-HDBK-263 is intended for voltage levels between 4000 and 15,000 Volts.

Presentationwise, DOD-HDBK-1686 specifies the minimum requirements but does not detail out the expectations of the requirement. DOD-HDBK-263 instead detailed out the expectations of the requirements as guidelines, covers the fundamental electrostatic theories, and its effect on semiconductors. The DOD-HDBK-263 is an excellent handbook covering ESD awareness, physics and applications. This handbook is intended to provide the guidelines to implement DOD-STD-1686.

ESD Handling Control program set up in a manufacturing facility shall include the following:

1. The functions to acquire and implement ESD Control program element should be established. The extent of the implementation of these requirements shall be based, upon the voltage sensitivity level of the most sensitive part applicable to the function.

2. Devices, assemblies and equipment shall be classified into Class 1 for 1000 Volts max. susceptibility, CLASS 2 for 1000 to 4000 Volts susceptibility level and CLASS 3 for 4000 Volts or more susceptibility level.

3. Design protection must be exercised in parts, assemblies and equipment cabinet terminals. Protective circuits may be needed to limit the sensitivity of parts assemblies and equipments.

4. Protected areas where ESDS items are handled should be limited to the lowest sensitivity level of the these items. As a minimum protected areas extends to 1 meter from the work area.

5. Handling procedures should be documented and implemented for all protective areas related to sensitivity of the device.

6. ESDS items in storage or transportation should be enclosed in ESD protective packaging, or contain shunting devices that short all pins.

7. When installing equipment, the protective covering should remain intact, until the required interconnecting cables and connector assemblies are completed.

8. Training in ESD awareness and proper handling are needed to applicable personnel who specify, acquire, design, manufacture, assemble, process, inspect, test, package, repair, rework, install or maintain ESDS items. Records of training is needed.

9. *Marking.* Deliverable documentation should identify the ESDS items in the documents while non-deliverable documentation should include or refer to documented protective handling procedures. Hardwares should be marked with approved ESD symbols located at a position, readily visible to personnel. The protective coverings should be similarly identified together with a caution note.

10. Quality assurance procedures must be established to ensure conformance to specified requirements which include certifying and periodical monitoring to assure integrity of protected areas.

11. Scheduled audits on ESD control program should be implemented and the results documented. The audits should cover the design and program reviews as follows:

    11.1 *Design reviews.* Design decisions relating to the ESD control program shall be presented at design reviews and shall include the following:

    a. Identification of Class 1 and Class 2 items;

    b. Results of classification circuit analysis for assemblies and equipment when applicable;

    c. Protective circuitry for parts and assemblies and equipment external interfaces;

    d. Marking of documentation including incorporation of protective handling procedures;

    e. Marking of hardware;

f. Problem areas relevant to meeting the requirements of DOD-STD-1686 and proposed corrective actions include tradeoffs.

11.2 *Program reviews.* Progress shall be assessed by the review of information such as:

a. General design, construction and maintenance requirements for protected areas;

b. Precautionary procedures used to control the handling of Class 1 and Class 2 items;

c. Methods and procedures for assuring adequacy of design of protective areas;

d. Quality assurance methods and procedures for monitoring the continued effectiveness of protective areas;

e. Quality assurance methods and procedures for performing audits of the ESD control program;

f. Contractor training program;

g. Protective covering, packaging and package marking for Class 1 and Class 2 items;

h. Problem areas in meeting the requirements of this standard and proposed corrective actions and tradeoffs.

12. Packing for deliveries have been discussed in the earlier section.

ESDS TESTING

1. ESDS CLASSIFICATION

ESDS Testing of devices employ the human ESD model. The requirements are specified in DOD-HDBK-1686, MIL-STD-883 method 3015. The test circuit have been earlier discussed by Dr. Kumar on ESD failure models.

For purpose of standardisation and interpretation, parts are considered to have failed the ESDS test if an electrically good part fails to meet one or more of the electrical parameters covered by the applicable part specification, or the part has changed by 10% or more where the electrical parameter has not been specified in the part specification.

The selection of pins combination is based on table 3 and if metallisation cross overs exists, the related pin combinations should also be tested. Test sequence should be done according to figure 12.1.

Note that ESDS testing on devices is a destructive test.

2. OTHER TESTING

2.1 Step Stress Testing

2.2 Latent Defect Testing

2.3 ESD Spark Testing

2.4 Lot Sample Testing

2.5 Assembly And Equipment Testing

2.6 Surface Resistivity Test

2.7 Decay Rate Test

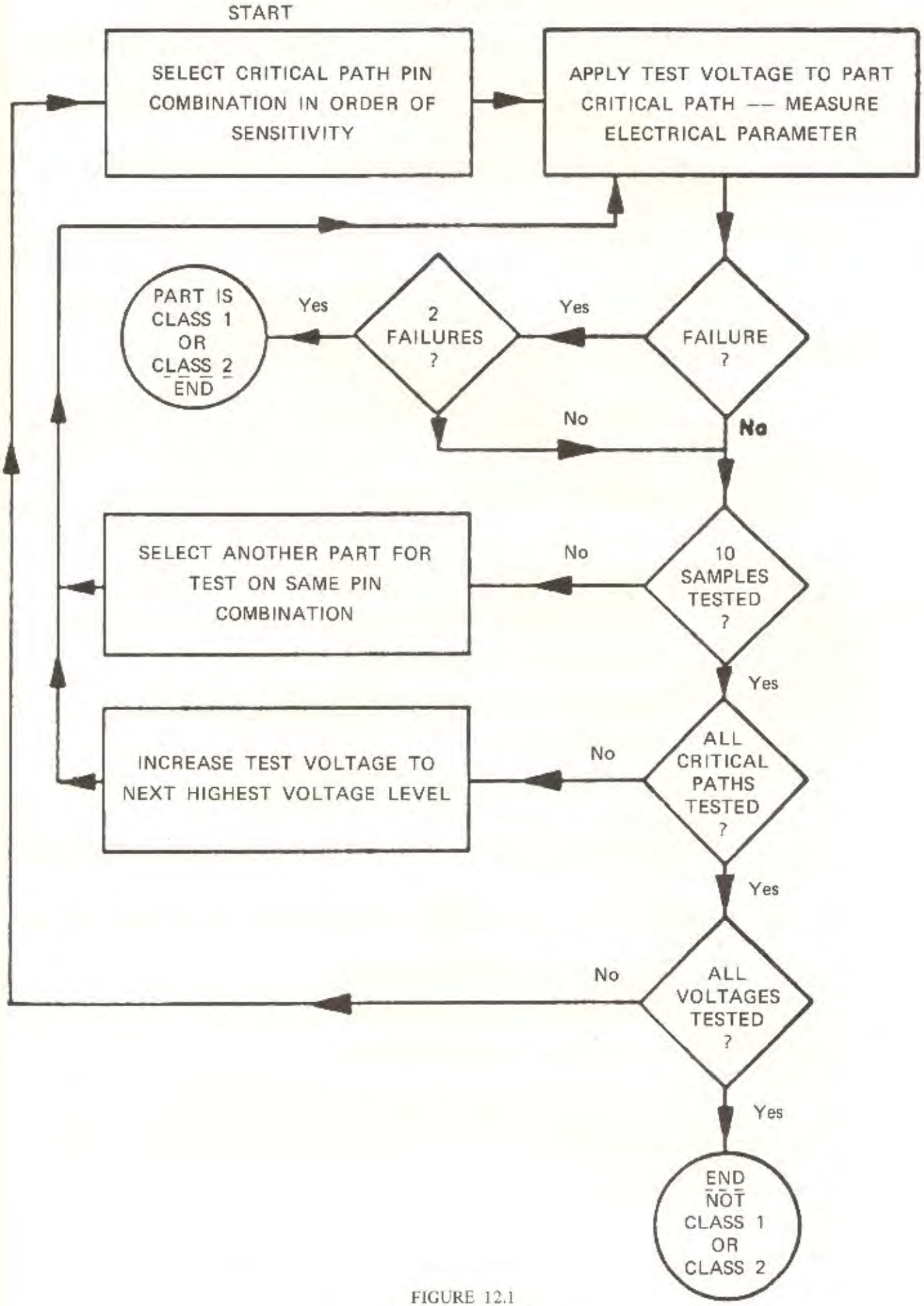


FIGURE 12.1
Classification testing

3. ESD TESTING EQUIPMENT

A detailed description of the ESD Testing Equipment requirements can be found in the IEC 801-2. A summary of the specification of the ESD Testing Equipment is as follows:

Test generator (E.S.D.)

The test generator consists, in its main parts, of:

- charging resistor,
- energy-storage capacitor,
- discharge resistor,
- power supply unit.

A simplified diagram of the E.S.D. generator is given in Figure 12.2.

The waveform of the pulse which is generated when the static electricity discharge takes place, is not formed in the generator prior to the discharge. The waveform depends on the kind of load.

The characteristics of the discharge current generated via a resistive load are given in Sub-clause 3.2.

3.1 *Characteristics and performance of the E.S.D. generator*

The characteristics of the E.S.D. generator are:

3.1.1 Energy storage capacitor (Cs): 150 pF ± 10%

3.1.2 Discharge resistor (Rd): 150 ± 5%

3.1.3 Charging resistor (Rch): 100 M ± 10%

3.1.4 Output voltage (1): 2 kV to 16.5 kV

3.1.5 Polarity of the output voltage: positive

3.1.6 Holding time (time during which the d.c. voltage, must be available at the tip of the test pistol): 5 s

3.1.7 Discharge, mode of operation (2): single discharge (time between successive discharges at least 1 s)

3.1.8 Rise time of the discharge current: see Sub-clause 3.2

3.1.9 Pulse duration (50%) of the discharge current: see Sub-clause 3.2

3.1.10 Peak value of the discharge current: see Sub-clause 3.2

Notes 1. – Open circuit voltage measured at the discharge energy storage capacitor.
2. – The generator should be able to generate at a repetition rate of 20 discharges per second for exploratory purposes only.

The generator shall be provided with means of preventing the emission of conducted interference from the generator via the power leads, either of pulse or continuous type so as not to disturb the E.U.T. The energy storage capacitor and the discharge resistor shall be placed as closely as possible to the discharge electrode. The dimensions of the discharge electrode are given in Fig. 12.3.

The earthing cable of the test generator shall be an insulated copper flexible strap, with the following dimensions:

- Length: 2000 mm (approx.)
- Width: 20 mm (approx.)
- Thickness: 0.1 mm (approx.)

Note. – A standard flat cable of the width specified above (with all the conductors connected in parallel) may be used instead of the copper strap. If round conductors are used, the minimum conductor size should be 22 AWG (about 0.7 mm diameter).

3.2 *Verification of the characteristics of the E.S.D. generator*

In order to make it possible to compare the test results obtained from different test generators, the following characteristics shall be verified:

3.2.1 Rise time of the discharge current at 4 kV : 5 ns ± 30%

3.2.2 Duration of the discharge current when above 50% amplitude at 4 kV : 30 ns + 30%

3.2.3 Peak value of the discharge current ± 30%: 9 A at 2 kV – 18 A at 4 kV
37 A at 8 kV – 70 A at 15 kV

The discharge of the E.S.D. generator shall be applied to a 2 ohm or less resistive load. The discharge electrode shall be approached to the load until the discharge occurs. The discharge circuit, including the earth connection shall be as short as possible.

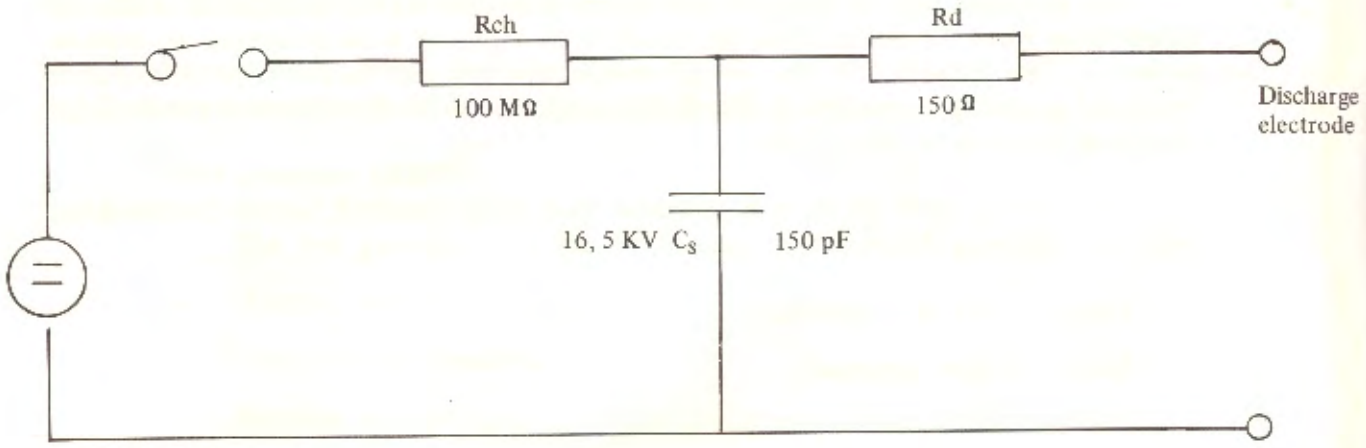


Fig. 12.2 Simplified Diagram of the E.S.D. generator

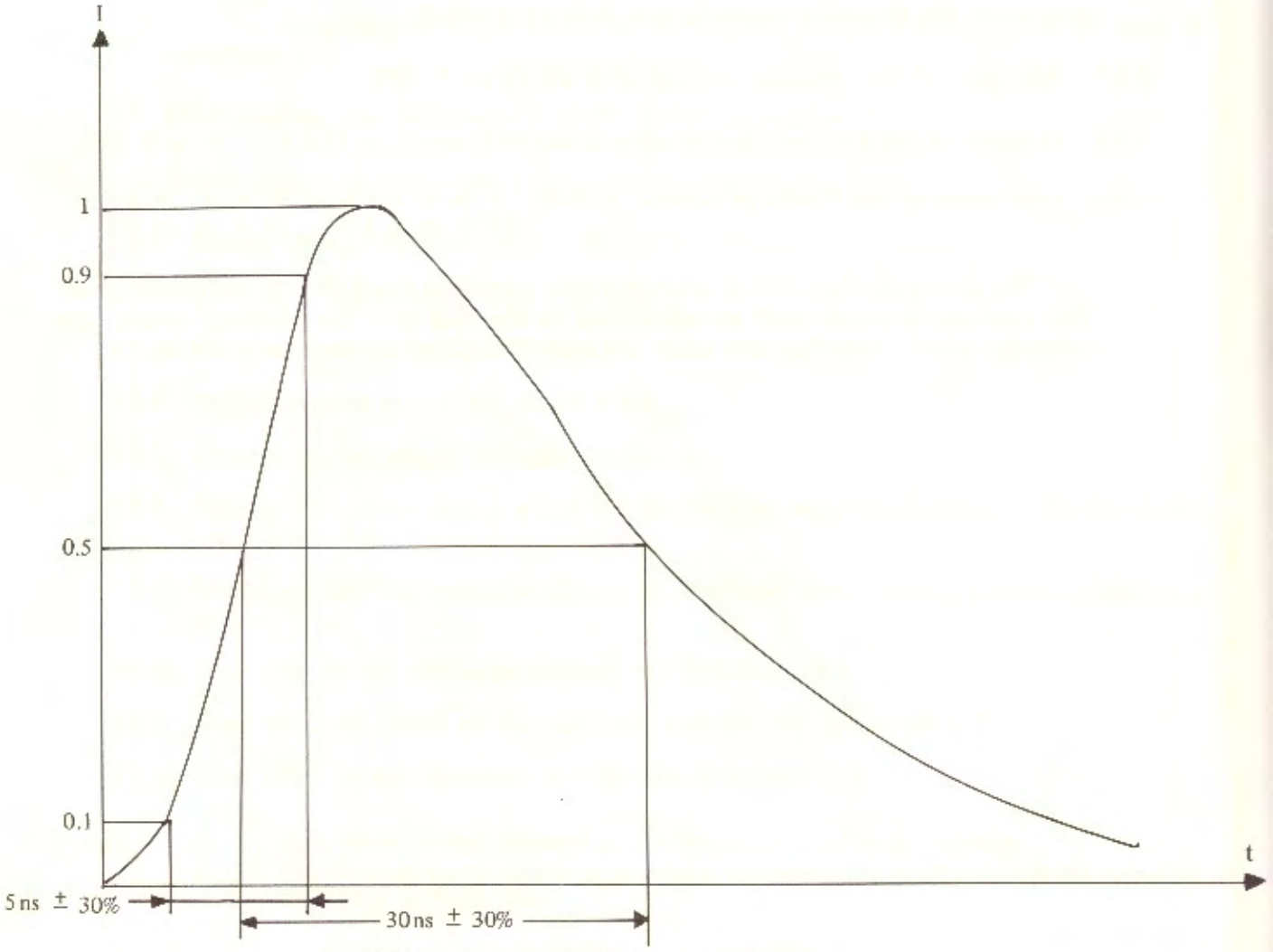


Fig. 12.3 Typical waveform of the output current of the E.S.D. generator

TABLE I. ESD control program

Functions Applicable to an Acquisition				Control Program Elements							
	See 5.1	See 5.2	See 5.3	See 5.4	See 5.5	See 5.6	See 5.7	See 5.8.1	See 5.8.2	See 5.9, 5.10	See 5.11
	Identification & Classification	Design Protection	Protected Areas	Handling Procedures	Protective Covering	Installation Site	Training	Marking Documen-tation	Marking Hardware	QA Provisions, Audits & Reviews	Packaging for Delivery
Design	X	X					X	X		X	
Manufacturing			X	X	X		X		X	X	
Inspection (Examination and Test)			X	X	X		X	X[1/]	X	X	
Packaging			X	X	X[2/]		X			X	X[3/]
Rework/Repair			X	X	X		X		X[1/]	X	
Failure Analysis			X	X	X		X			X	
Training Courses							X			X	
Field Installation						X[4/]					
Field Maintenance/ Test			X	X	X		X			X	

1/ If not previously performed.

2/ Internal to contractor's facility.

3/ External to contractor's facility.

4/ For a shipbuilding contract, unless otherwise specified in such contract, the installation site element is the only element of this table that applies to ships and shipyards.

TABLE 2: ESD TRAINING GUIDELINES

Type of Personnel	Training Course Outline Section								
	A	B	C	D	E	F	G	H	I
	ESD Control Program	Principles of Static Electricity	Electrical and Electronic ESDS Items	ESD Protective Materials and Equipment	Protected Areas/Grounded Work Benches	ESD in Design	Failure Analysis Techniques	Handling Precautions and Procedures	Packaging and Shipping of ESDS Items
Program Manager	X	X							
Engineering	X	X	X	X	X	X	X	X	X
Acquisition Personnel	X	X	X	X					X
Quality Control Personnel	X	X	X	X	X	X	X	X	X
Field Engineer, Installation and Maintenance		X	X	X	X			X	X
Production Operators and Technicians		X	X	X	X			X	X
Stockroom and Kitting Personnel		X	X	X	X			X	X

TABLE 3: PIN COMBINATIONS FOR ESD TESTING

Part Types	Pin Combinations
All parts	• All pins tied together (+) to top center of case (–) • All pins tied together (–) to top center of case (+)
Resistors	• Terminal (+) to terminal (–)
Diodes	• Anode (+) to cathode (–) • Anode (–) to cathode (+)
Transistors	• Emitter to base* • Base to collector*
Digital Microcircuits	• Input (+) to common (–)** • Output (–) to common (+)** • Input (+) to output (–) • V+ (–) to common (+)
Linear Microcircuits	• Input (+) to common (–) • Input (+) to input (–) • Output (–) to common (+) • V+ (–) to common (+)
MOS FETs and JFETs	• Gate to source* • Gate to drain*

* Both polarity (+) to (–) and (–) to (+)

** Common – For NPN technology microcircuits common is the most negative terminal (i.e., V– or GND); for PNP technology common is GND.

13. DEMONSTRATION: GENERATION AND CONTROL OF TRIBOELECTRIC CHARGES

Static electricity has been doing its dirty work since the day of the caveman, when lightning caused direct injuries, damage and started life-threatening fires. And today, when man has progressed from the cave to his high tech space capsule, static-induced malfunction of a tiny electronic device could also cause a life threatening situation.

Static electricity has long been a problem in many industrial and commercial operations and is a serious hazard especially in explosive atmospheres and in areas where flammable solvents or materials are present.

Not only is the sudden discharge, or arcing, of static electricity responsible for fires and explosions, but it also causes losses in the millions of dollars to manufacturers in machinery down time and lost man-hours and in product loss particularly in the semiconductor and electronics industries where static sensitive components are degraded or destroyed by only a few volts of static electricity. For the user of sophisticated electronics, static causes loss of memory, false inputs, etc, to electronic memory equipment such as computers, data terminals and word processors.

The effects of static electricity in manufacturing processes have become more and more of a problem with the widespread use of synthetic materials and high speed machinery. Some plastics, for example, when travelling through a machine, may develop static charges of several thousand volts. These highly charged materials are sometimes attracted to machine rollers or guides causing jams and even damage to the machinery. This same highly charged material, if rewound onto a large roll as in a slitting and rewind converting operation, can become a huge capacitor, capable of storing in excess of 50,000 volts of static electricity. This highly charged "capacitor" could cause uncomfortable shocks to operators, even burns, or injury due to physical reaction from receiving a shock. The "capacitor" could arc to a nearby conductor and produce a strong arc several inches long, easily causing a fire or explosion if in the right situation.

In critical areas such as food and drug packaging, semiconductor and biomedical products manufacturing, and virtually any process requiring clean room procedures or simply a clean product, static becomes a problem. Any part or material supporting a static charge will attract contamination whether it be in the form of microscopic size dust particles, or dust and chips from machining.

Most static related problems, however simple or complex they may seem, can be solved once the problem is addressed, analyzed and the proper control methods are implemented and adhered to.

THEORY

In order to be able to analyze static problems and determine the proper solutions or methods of neutralization, it is important to understand the physical and electrical principles involved in the generation of static electricity.

The molecular theory of matter structure states that each molecule of a body is composed of positive and negative charges. The positive charges are contained in the nucleus of the molecule, while the negative charges or electrons, are free to orbit around the positively charged nucleus. In a molecule that is neutral or uncharged, the sum of the negatively charged orbiting electrons is equal to the sum of the positive charges in the nucleus. Any matter composed of all neutral molecules is also neutral.

Under certain conditions, some molecules do not have enough force or attraction between the positive nucleus and the negative orbiting electrons to keep all electrons in orbit. In this case, the outermost orbiting electrons which are called valance electrons, tend to be attracted to an adjacent molecule with a greater force of attraction, leaving an excess of positive charges in the nucleus. The molecule thus becomes positively charged. In the reverse, some molecules tend to pick up additional electrons causing an imbalance, and resulting in a negatively charged molecule. Any matter with

excess negative molecules becomes negatively charged, and conversely, matter with excess positive molecules becomes positively charged.

Objects or materials can become charged by frictioning, or more simply, just contact and separation of two materials. When two objects or materials are brought into intimate contact, the valance electrons nearest the surface of the material, move freely about, from molecule to molecule, from material to material, until they attach themselves to stronger nuclei. Upon separation of the materials, one material looses electrons and becomes negatively charged. As the pressure of speed of contact and separation or friction increases between the two materials, the static charge voltage increases.

Another means by which an object or material may become charged is by induction. A highly charged object results in a static field around the object. If an isolated or ungrounded conductive object enters into this static field, it too will become charged, but of the opposite polarity. This sets the stage for a possible electrostatic discharge to some other conductive object, which could result in an arc of sufficient energy to ignite combustribles or destroy sensitive electronic components. If the conductive object with the induced charge is then removed from the field, it will return to its original state.

INSULATORS AND CONDUCTORS

When dealing with static electricity, the types of materials involved must be considered. Materials are divided into two basic classifications: conductors and insulators. Within a conductor, electrons move freely about throughout the entire body. Therefore, when an ungrounded conductor becomes charged, the entire volume of the conductive body assumes a charge of the same potential and polarity. A charged conductor can be neutralized simply by connecting it to earth ground, since ground is virtually an infinite source and receptacle for electrons. If a conductor is positively charged and connected to ground, the required quantity of electrons will flow from ground to the conductor until the conductor becomes neutral. In the reverse, if the conductor is negatively charged and then connected to ground, the excess electrons will flow to ground until the conductor becomes neutral.

An insulator reacts much differently to static electricity and cannot be neutralized by simple grounding techniques as can conductors. Within an insulator the flow of electrons is very limited. Because of this an insulator may retain several static charges of different potentials and polarities at various areas on its surface. Connecting the insulator to ground will not result in an exchange or flow of electrons as is true of conductors, therefore other means must be used for neutralizing static on insulators.

TWO BASIC METHODS FOR NEUTRALIZING STATIC

There are two basic methods for neutralizing static: the conductivity method and the replacement method. As previously mentioned, a conductive object can be neutralized by connecting it to earth ground. As long as the conductor remains grounded, static charges cannot develop.

CONDUCTIVITY METHOD

An insulator, if it can be made conductive, can also be neutralized when grounded. An insulator can be made somewhat conductive by one of the following methods: humidification, antistatic chemical coatings, internal antistatic agents and carbon loading.

Some materials which are hygroscopic have the ability to absorb moisture when exposed to high humidity conditions. In this case the material becomes sufficiently conductive to bleed off some static charges. With nonhygroscopic materials, the level of humidity required for effective static charge dissipation, however, would not be practical for most manufacturing applications.

Antistatic chemical coatings are applied to nonconductive objects by spraying, wiping or dipping, and forms a conductive surface which dissipates static charges. The chemical itself does not make the surface conductive, but actually absorbs moisture from the air which collects on the surface and forms somewhat of a conductive layer.

Internal antistats are chemicals which are mixed in with plastics at the time of molding or extrusion. These antistats continue to migrate to the surface and work on the same principle as the antistatic coatings.

Carbon can be added to plastics prior to molding or extrusion to form carbon-loaded conductive plastics. This process, as well as the use of internal antistats, is used more in the manufacture of products for controlling static electricity and not necessarily as a fix or remedy for static problems encountered during manufacturing processes.

REPLACEMENT METHOD – IONIZATION

If the missing electrons in a positive charged material can be replaced, or if a negative charged material can be made to absorb positive ions, the material can be neutralized. This process is made possible through ionization, which is the splitting of air molecules into positive and negative charges. An ionizing device emits quantities of negative and positive ions in the vicinity of the static charged object. Since opposite charges attract, the charged object takes on a sufficient number of negative or positive ions, depending upon which is required for neutralization. This ionizing device acts as an infinite source for negative and positive ions.

METHODS OF IONIZATION:

There are three basic types of equipment available for producing ionization; electrically powered high voltage static neutralizing equipment, nuclear powered equipment and induction-type neutralizers.

An electrically powered static neutralizer consists of one or more ionizing points to which a high voltage is applied in close proximity to a ground reference. The high voltage field occurring between the ionizing point and the ground reference, ionizes the air. When a charged material passes within this field it becomes neutral. Electrically powered static neutralizing devices are available in many different configurations including X-Proof designs for hazardous locations. The term "shockless," when referring to electrically powered equipment, means that the ionizing point is capacitively coupled to the high voltage source, thus limiting current at the point to a very level. Direct contact with the point will not result in a shock sensation and since energy is very low, arcing will not cause ignition of flammable materials. Nonshockless designs usually offer greater efficiency in certain applications involving extremely high charges or high speed materials. In this equipment the high voltage source is coupled directly to the ionizing point. Direct personal contact with the point will result in an uncomfortable shock sensation, and sufficient energy is available to possibly cause ignition of flammable materials. When specifying equipment, shockless or nonshockless designs should be selected depending upon the individual application.

Nuclear powered static eliminators use elements such as polomium or radium, which are encapsulated in ceramic beads and affixed to the neutralizing devices. These materials bombard the surrounding air molecules with high-speed alpha particles which cause ionization. Nuclear equipment can be used in hazardous areas and does not require electrical connections. However these devices can only be leased and must be replaced on a yearly basis.

Induction type equipment, even though it is not externally powered, uses the high voltage principle of ionization. These units are usually in a straight bar configuration with a series of ionizing points of tufts of wire connected to a grounded metal bar. The high voltage required for ionization is actually the high voltage static charge on the material itself. As the material passes the induction bar, the high voltage field associated with the static charge on the material seeks a ground reference which is the series of points on the bar. This ionizes the air sufficiently to aid in neutralization, but cannot always achieve sufficient neutralization to solve the problem.

With induction bars, the higher the potential on the charged material, the greater the ionization. This also works in reverse, however. As the charge on the material decreases, so does the ionizing efficiency until it reaches a threshold level where ionization stops. After this point, other means such as electrically powered or nuclear powered equipment must be used.

DEMONSTRATION NO. 1: TO DEMONSTRATE STATIC CHARGES ON A NON-CONDUCTIVE MATERIAL AND HOW IT CAN BE ELIMINATED

EXPLANATION	ACTION
1. Almost any material can pick up a static charge. If that charge is allowed to build, it can disable micro-electric components, clog automatic machinery or contaminate hospital rooms and aerospace research lab. Nearly all materials can pick up some kind of electric charge: hands and hair, silk, aluminium, lead, paper, nylon, wood, especially the non-conductive materials.	
2. We can demonstrate and prove the presence of static charges on a non-conductive material like the nylon cloth by using the electrostatic locator to measure/locate the static charges.	Use the electrostatic locator to locate static charges on the nylon cloth.
3. However if an insulator or non-conductive material is made conductive, then it can be neutralized by grounding. One of the methods to make the insulator conductive is by applying anti-static chemical coatings to the insulator/non-conductive object by spraying, wiping or dipping. As such, a conductive surface is formed which will dissipates static charges.	
The chemical itself does not make the surface conductive, but actually absorbs moisture from the air which collects on the surface and forms somewhat of a conductive layer.	Spray anti-static solution on nylon cloth and measure the static charges with electrostatic locator.
However, this is only a temporary measure to bleed away the static charges.	After some time measure the cloth with the electrostatic locator.
4. Based on the principle of conductivity method for neutralizing static, there are various line of conductive products/materials which prevent static build-up on personnel, work areas, equipment and parts. For example, we will show you the conductive/ anti-static mat which can safely maintains parts and materials at ground potential during manufacturing, packaging and shipping.	Measure the conductive mat with the electrostatic locator to show no static charges.

DEMONSTRATION NO. 2: TO DEMONSTRATE THE GENERATION OF STATIC CHARGES BY SEPARATION OF NON–CONDUCTIVE MATERIAL AND HOW IT CAN BE ELIMINATED

EXPLANATION	ACTION
1. The continued separation of non-conductive surfaces (particularly those made out of plastic) can cause most static build up. When the non-conductive surfaces separate, electrons are pulled from the surface leaving it electrically charged. Since the surface is often a poor conductor, it holds its charges. Therefore the charges remains static.	
2. Through friction, these separation occur rapidly and the more rapid the separation, the greater the static build-up. Examples can be seen in: UNROLLING FILM MOVING BOXES FILLING PLASTIC BAG MERELY WALKING ACROSS A FLOOR All these can build-up static charges.	
3. We will show you that static charges can be generated by merely walking on, say, vinyl material.	Use electrostatic locator to show minimum static on vinyl material. Demonstrator walk over vinyl material. Measure with electrostatic locator to prove increase in static charges.
4. The solution to eliminate static build-up on personnel, work area, equipment is to use: – conductive flooring – conductive shoes – conductive uniform – conductive gloves – wrist strap	Use electrostatic locator to check for zero charges on those conductive items.
5. The separation of non conductive surfaces, especially where a lot of friction are involved can build up static charges. For example the constant use of the tacky mat will increase static charges.	Measure the tacky mat with electrostatic locator. Demonstrate to clean shoes on tacky mat. Measure the mat to show increase in static in charges.
6. However, if the tacky mat is made conductive, then it can become neutralized when grounded. We would like to show you the tacky mat that are carbon-loaded to prevent static build-up.	Measure the antistatic mat. Demonstrator to clean shoes on stat-trak. Measure the Stat-Trak to show no increase in static charges.

DEMONSTRATION NO. 3: TO DEMONSTRATE BUILDING OF STATIC CHARGES USING AN ACRYLIC AND METAL PLATES AND HOW IT CAN BE ELIMINATED.

EXPLANATION	ACTION
1. Sometimes when an insulator and a metal rubbed against each other (ie. friction occurred) and then separated, static charges are build-up on both the insulator and metal. For example: in this demonstration the negative charges are build-up on the acrylic plate and positive charges on metal. It shows that sometimes even static charges are build-up on the conductive material.	Rub both acrylic and the metal together and separate them. Measure with electrostatic locator.
2. By using the ionising blower, the air is ionized ie. the air particle is broken into positive and negative ions. When the acrylic plate (negative charge) is subject to the ionized air, the plate will absorb positive ions and become nuetralized. Conversely, for the metal plate. Therefore, the charged insulator and metal can neutralized easily.	Use ionizing blower to neutralize the acrylic and metal piece. Measure with electrostatic locator to show charge had been neutralized.

DEMONSTRATION: EFFECT OF STATIC CHARGES ON SEMICONDUCTOR DEVICE

Introduction

Damage to sensitive components by manual handling is a well known fact, but yet in our local condition there is a belief that the damage due to charged human person is "non-existence". This misconception arises from the understanding that humidity in the tropic is high and therefore the ESD threat is reduced. However since most tests or fabrications of electronic devices are done in controlled conditions (temperature and humidity), the ESD problem encountered in dry and cold countries is no means a lesser problem in Singapore.

The workshop sessions with some practical hand-on will show that sensitive devices can be degraded or damaged with the presence of ESD.

Objectives

1. To demonstrate the presence of ESD on human body

2. Demonstrate the "zapping" & degradation of devices

   a) Devices in an anti-static packages
   b) Devices mounted on board
   c) Devices in anti-static shipping tube

3. To show the different failure modes

4. To observe actual damaged spot

The device for demonstration is a 3N157 MOSFET. The device is used in a smoke detector, this P-channel FET acts like a normally open switch. According to the manufacturer, the device will turn on with current (Ids) of 10 microamp when a gate voltage (Vgs) of -1.5V to -3.2V is being applied. The voltage between drain and source is -15V (Vds).

In the workshop we shall concern ourselves with the day to day ESD problem arises with human contact and sensitive devices. We shall attempt to show that devices are degraded and finally damaged with increase of level of static charge applied to the devices through the human body.

By inspecting the result by curve tracer and optical scope we shall try to identify and interprete the different failure modes and thereby show that ESD will cause sensitive devices to fail differently. differently.